# A MANIFESTO FOR FUTURE GENERATION HETEROGENEOUS COMPUTING: RESEARCH DIRECTIONS

A PREPRINT

**Karim Djemame, Richard Kavanagh**
School of Computing
University of Leeds
Leeds, UK
{K.Djemame,R.Kavanagh}@leeds.ac.uk

**Juan Fumero, Christos Kotselidis, Athanasios Stratikopoulos**
Department of Computer Science
University of Manchester
Manchester, UK
{fist.last}@manchester.ac.uk

**Christoforos Kachris**
ICCS
InAccel
Athens, Greece
kachris@microlab.ntua.gr

**Iakovos Mavroidis**
Telecommunication Systems Institute
Chania, Crete
iakovosmavro@gmail.com

**Ioannis Papaefstathiou**
Synelixis Solutions SA Athens, Greece
ygp@synelixis.com

**Sokol Kosta**
Department of Electronic Systems
Aalborg University
Copenhagen, Denmark
sok@es.aau.dk

**Manos Pavlidakis, Stelios Mavridis, Nikos Chrysos, Angelos Bilas**
Department of Computer Science
Institute of Computer Science,
Foundation for Research and Technology-Hellas, Greece
{manospavl, mavridis, nchrysos, bilas}@ics.forth.gr

**Alberto Scionti, Olivier Terzo, Francesco Lubrano**
Advanced Computing and Applications (ACA)
LINKS Foundation, Italy
{alberto.scionti, olivier.terzo, francesco.lubrano}@linksfoundation.com

**Paolo Burgio**
High-Performance Real-Time Lab (HiPeRT)
University of Modena and Reggio Emilia, Italy
paolo.burgio@unimore.it

**Raffaele Montella**
Department of Science and Technologies (DiST)
University of Naples "Parthenope", Italy
raffaele.montella@uniparthenope.it

June 25, 2020

## ABSTRACT

Hardware in various environments such as High Performance Computing, the Internet of Things and Embedded Systems has become heterogeneous in order to improve computational performance. Customising the hardware for particular application domains as well as the use of accelerators such as GPUs, TPUs, DSPs, FPGAs is attractive as it can lead to performance improvements of up to three orders of magnitude compared to general-purpose processors. Recent technological developments and paradigms in compilers, profilers, and run-time systems are creating new opportunities for heterogeneous computing. However, these are also posing several new challenges and creating the need for new approaches and research strategies, as well as the re-evaluation of the models that were developed to address issues such as application models, programming models, middleware, scalability, security and sustainability. The proposed paper identifies the major open challenges in heterogeneous computing, emerging trends, and impact areas. It then offers a future research agenda, thus helping in the realisation of Future Generation Heterogeneous Computing.

***K*eywords** Heterogeneous Architectures · Parallel Programming Models · Future Trends

# 1 Introduction

Information and Communication Technology (ICT) has tremendous potential to improve safety, convenience, and comfort in our daily lives. There is a paradigm shift in areas such as High Performance Computing, the Internet of Things (IoT) and Embedded Systems in which their deployment and operation demand the use of hardware platforms that are able to manage the steadily increasing requirements in computing performance, energy efficiency, security and the adaptability.

The exploitation of the capabilities offered by customised heterogeneous hardware such as heterogeneous CPU+GPU chips, heterogeneous multi-processor clusters, Multi-Processor System on Chip (MPSoC), Field-Programmable Gate Arrays (FPGA) and Application-Specific Integrated Circuits (ASIC), all of which with various memory hierarchies, size and access performance properties, becomes attractive.

However, the design and development of software architectures for applications to execute on a set of heterogeneous hardware devices to achieve the expected performance is complex. For example, mapping software components onto heterogeneous hardware processing devices must not only consider performance, but other factors such as energy consumption and data transfer as well.

## 1.1 Motivations and Goals of the Paper

Throughout the evolution of heterogeneous computing and its increasing adoption, not only have the hardware aforementioned architectures advanced and new ones emerged, but also the technologies in which this paradigm is based (e.g., virtualisation) have continued to progress. Moreover, there has also been a rise in the type and number of specialised computing services that aid industries in creating value by being easily configured to meet specific business requirements. Examples of these are emerging, easy-to-use, often Cloud-based services include Amazon EC2 F1 FPGAs instances to enable delivery of custom hardware accelerations [1], and Google Tensor Processing Unit (TPU), a custom-designed machine learning ASIC [2].

As the impact of heterogeneity on computing tasks is rapidly increasing, innovative architectures, algorithms, and specialised programming environments and tools are needed to efficiently use these mixed and diversified parallel architectures. One of the major challenges to exploit their benefits, in data centric and emerging domains, is the complexity in designing and maintaining a software stack that can deliver such benefits. Developers need to fully understand the nuances of different hardware configurations and software systems (both rapidly evolving), as well as consider additional difficulties in performance, security mixed-criticality and power consumption resulting from the heterogeneous system [3].

The adoption of heterogeneous computing will therefore continue to increase and support for related emerging models and services is of paramount importance. The vendor ecosystem will continue evolving, with new heterogeneous hardware leading the way and a strong increasing adoption rate for non-x86 processors, such as FPGAs , among others. According to Allied Market Research [4], the FPGA market was valued at $3.92B in 2014 and is expected to reach up to $7.23B by 2022, at a CAGR of 7.41% between 2016 and 2022. Moreover, Intel expects a CAGR of 7% between 2014 and 2023 reaching revenues of $8.9 billion at the end of the forecast period. The GPU market size is expected to reach $157.1 billion by 2022, growing at a CAGR of 35.6% during the period, 2016-2022.

This extensive usage of heterogeneous computing in various emerging domains is posing several new challenges and is forcing a rethink of the research strategies to address issues such issues such as programming models, resource management, scalability, and security for the realisation of next-generation heterogeneous computing environments. This comprehensive manifesto brings these advancements together and identifies open challenges that need to be addressed for such realisation. We envision that identified research directions get addressed and will impact the next generations of heterogeneous computing technologies, infrastructures, and applications.

The manifesto first discusses major challenges in heterogeneous computing, investigates their state-of-the-art solutions, and identifies their limitations. It discusses the emerging trends and impact areas, that further drive heterogeneous computing challenges. The manifesto then offers comprehensive future research directions in the heterogeneous computing horizon. Figure 1 illustrates the main components of the heterogeneous computing paradigm and positions the identified trends and challenges, which are discussed further in the next sections.

The rest of the paper is organised as follows: Section 2 discusses the state-of-the-art of the challenges in heterogeneous computing and identifies open issues. Section 3 discusses the emerging trends and impact areas related to the

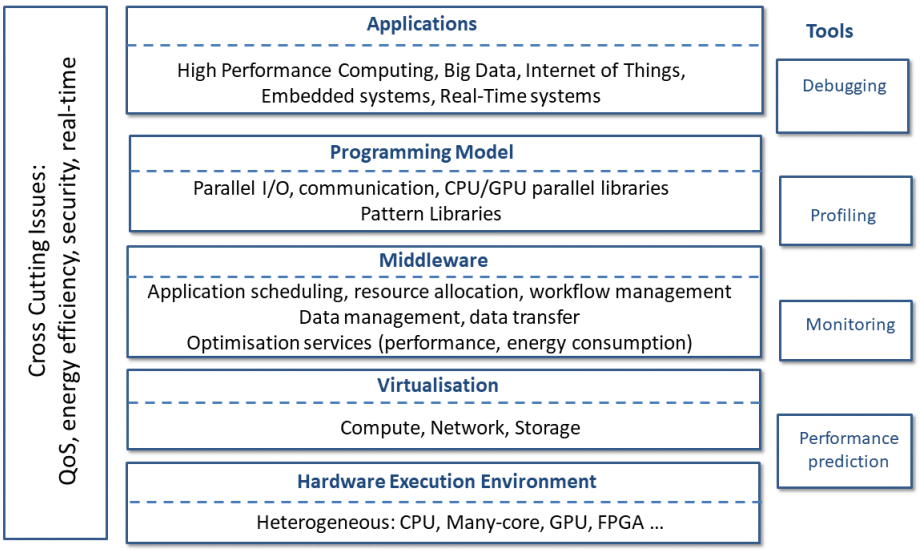


Figure 1: Components of the Heterogeneous Computing Paradigm

heterogeneous computing horizon. Section 4 provides a detailed discussion about the future research directions to address the open challenges of heterogeneous computing. Section 5 concludes the manifesto.

## 2 Challenges: State-of-the-Art and Open Issues

Heterogeneous Computing is extensively utilised in hosting a wide variety of applications, e.g. Cyber Physical Systems, which are deployed in many different contexts and application domains such as healthcare, autonomous vehicles, traffic management, edge video orchestration, and industrial IoT. It still poses several challenges such as issues with hardware heterogeneoty, programming models heterogeneity, resource management, and sustainability among others. Over the past decade, these challenges were systematically addressed and the state-of-the-art in heterogeneous computing has advanced significantly. However, there remains several issues open. The rest of the section identifies and details the main challenges in heterogeneous computing and their state-of-the-art, along with the limitations driving their future research.

### 2.1 Applications and Software

Nowadays there exists a guide range and very specialised set of applications, such as Machine Learning, Deep Learning, Big Data, Cyber Physical Systems (CPS), Internet of Things (IoT), connected smart objects, High Performance Computing (HPC), mobile computing, wearable computing. The strict requirements for fast processing and the high demand for those applications mean that software written for those application domains is quite likely to be executed on heterogeneous hardware, such as GPUs, FPGAs, or even custom designed hardware such as Tensor Processing Units (TPUs) for deep learning. However, for these applications to fully exploit the benefits of heterogeneous platforms, there is a need to design more flexible software abstractions that facilitate programming while increasing productivity and rapid changes of computer software.

Those abstractions require the knowledge, from the programmers' perspective, about parallel design patterns, such as Map/Reduce [5] and structured parallel skeletons [6] such as fork/join, stencils, scan, gather and scatter. Those conform the core set of algorithmic skeletons to implement by programmers that want to use heterogeneous and parallel hardware. There are many frameworks and compute libraries that gather all these algorithmic skeletons in such as way that programmers only have to worry about what problem to solve, and not how to write efficient code.

However, every time that new heterogeneous hardware come along, such as the use of FPGAs, or custom designed hardware, knowing the skeletons to use is not enough. This is due to the programming models and abstraction are quite far from the actual hardware. In some sense, this is good. However, when the application requirements are peak performance and very low power consumption, developers needs to take care of every little detail regarding the heterogeneous computing architecture, such as use of registers, how to decrease latency, how to increase throughput, etc.

This strategy makes software much harder to maintain and evolve. Therefore the real challenge regarding computing software applications is how to find the balance between productivity and compliance with the requirements such as low energy consumption and high-performance.

### 2.2 Hardware Heterogeneity

Nowadays, practically all computing systems contain some sort of heterogeneous hardware, such as dedicated GPUs, integrated GPUs inside the main CPUs, and new custom designed hardware. This new heterogeneous hardware are contained in multiple devices that society use in daily basis. This ranges from mobile devices, to tablets, laptops and even data centers, which also include Field Programmable Gate Arrays (FPGAs) to increase performance while decreasing energy consumption. This Section presents the challenges that accompanies this new heterogeneous hardware.

Due to the heterogeneous hardware present in modern computing systems, applications will require efficient support from those heterogeneous hardware, irrespective of their application domain: embedded, mobile, cloud, big data, machine and deep learning, etc. The new hardware should guarantee the application requirements, such as performance for real-time and safety-critical applications. Heterogeneity hardware is considered at two levels: 1) *Macro level*: networks of distributed computers (clouds, clusters), composed by diverse node architectures (single, multi-core), are interconnected with potentially heterogeneous networks, and 2) *Micro level*: deeper memory hierarchies (main, cache, disk storage, tertiary storage) and various accelerator architectures (fixed and programmable, e.g., GPUs, and reconfigurable, such as FPGAs).

At macro level, cloud computing has become the dominant model for end-users to access centrally managed computational resources. For example, Amazon Web Services and Microsoft Azure provide users with access to a homogeneous set of commodity hardware, with details of the hardware obscured through virtualisation. If cloud users are to be able to take advantage of the performance and efficiency of heterogeneous computing, the cloud software stack must recognise and support this heterogeneity. This is challenging due to the complexity of the software stack.

At micro level, one promising accelerator architecture is the employment of energy-efficient reconfigurable resources (in the form of FPGAs) tightly integrated with conventional CPUs. One of the main problem with this approach is that today's FPGA tools and programming environments are usually optimised for accelerating a single application or task on a single FPGA device.

### 2.3 Heterogeneous Programming Models

One of the most important challenges to address with heterogeneous architectures is their programmability. Hardware architectures (such as multi-cores, GPUs or FPGAs) require specific programming models. Notice that in this paper, we borrow the term *programming model* from McCormick et al. [7] that can be seen as an abstraction to facilitate development of diverse and heterogeneous hardware. This term is often confused with the programming language itself. We believe that a programming model is independent of the programming language, in which data representation and execution control differ from the base programming language, and, therefore, need to be explained to understand how programs are executed on heterogeneous hardware.

We can classify heterogeneous programming models in the following categories:

- Directive-based programming models.
- Explicit parallel programming models.
- Domain specific embedded programming models.
- Reconfiguration hardware programming models.

This section provides an overview of each of these heterogeneous programming models and shows the trade-offs between them.

**Directive-based parallel programming** Popular and mainstream programming languages, such as C/C++ and Java, have no language abstractions to express parallelism, or in other words: parallelism is not part of the programming model of the base language. The idea behind directives, or code-annotations, is that programmers can execute legacy and sequential code, created for a single thread execution, on heterogeneous and parallel devices such as GPUs and FPGAs. This strategy splits the code at least into two main parts: the code that is executed on the host part (i.e., the main CPU), and the code that will be executed on the device (e.g., a GPU or an FPGA). When the code is executed on a device, the execution and data-flow diverges from the base programming language.

Listing 1: Sketch of code that shows a vector addition in OpenACC.

```
1 #pragma acc kernels copyin(a[0:n],b[0:n]), copyout(c[0:n])
2 for(i = 0; i < n; i++) {
3     c[i] = a[i] + b[i];
4 }
```

Listing 2: Sketch of code that shows a vector addition in OpenMP 4.5.

```
1 #pragma omp target data map(to:a[:n],b[:n]) map(from:c[:n])
2 {
3   #pragma omp target teams distribute parallel for schedule(static, 1)
4   for(i=0; i<n; i++) {
5     c[i] = a[i] + b[i];
6   }
7 }
```

The main two standards are OpenACC [8] and OpenMP 4.0 [9], in which developers add annotations (or `pragma directives`) to their existing loops to inform to an underlying compiler that some regions of the code can be parallelized. Because annotation are not actually part of the syntax's programming language, they can be ignored. Instead, the preprocessor tool is the responsible for analysing the annotations and injects the corresponding runtime calls that make the code to be parallelized. To illustrate the use of directives, Listing 1 shows an example of a sequential C code for computing vector-addition computation using OpenACC. Observe that the loop that performs the vector-addition is annotated with a set of OpenACC directives, such as `kernel`, to indicate that the following `for-loop` can be offloaded to a heterogeneous device; and the directives `copyin` and `copyout`, that indicates which variables need to be copied from the host (the main CPU), to the target device (e.g., a GPU). Note also that those directives can be considered low-level, which means that developers are responsible for identifying the potential parallel kernels that are good fit for running on heterogeneous hardware, and annotate all parameters needed to make it work.

Similarly, OpenMP 4.0 introduced a set of new directives and annotations that extends the multi-core shared memory programming to heterogeneous hardware. Listing 2 shows the same example of how to perform a vector addition but using OpenMP 4. One of the main differences comparing to OpenACC is that OpenMP 4 is much more verbose. This is due to the fact that OpenACC was created with the GPU execution and data model in mind. However, the origins of OpenMP were to support a standard for parallel computation on shared memory machine for multi-core and multiple CPUs. Therefore OpenMP 4 needs to keep compatibility of legacy OpenMP applications. If we break down the line 1 in Listing 2 we see that the target directive is used. This indicates that the following region (`for-loop`) can be offloaded to an accelerator (that includes a multi-core CPU or a GPU). Then it specifies how data should be seen by the host. We indicate a copy from host to the target device the variable `a` and `b` and then a copy from device to host. The second `pragma-directive` in line three defines how threads are organized and executed on the target device. As the reader can see, OpenMP 4 is lower-level compared to OpenACC to express the same computation. OmpSs [10] is also another parallel programming model based on directives that makes use of multi-core systems, GPUs and FPGAs and it is built on top of OpenMP 4, and it follows similar approach than OpenMP 4 for annotating sequential C-programs to execute on heterogeneous devices.

All of these directive-based programming models use C/C++ and Fortran programming languages as the main targets for expressing applications that are normally used in the context of high-performance computing (HPC) and shared-memory machines. However, these models can be easily integrated into distributed memory systems that uses, for example message passing, such as MPI [11], map-reduce computation [12, 6] or reactive programming [13], just to name a few.

The main advantages of directive-based approach is that the main C/C++ or Fortran code remains almost the same as the sequential version, and annotations are taken as hints by the compilers to generate runtime calls that can compile a C-code into a parallel code suitable for heterogeneous devices (e.g., a GPU). The main disadvantage is that, although their simplicity, they require expertise from the user's perspective to efficiently generate and accelerate code on the heterogeneous device. One typical example is OpenMP, as we showed in Listing 2, which requires a lots of directives and loop-annotations in the right order to be able to achieve high-performance using GPUs.

**Explicit Heterogeneous Programming Models** As an alternative for annotating sequential code, there are the explicit and new heterogeneous programming models that extend the existing programming languages such as C and C++. Depending on the target device, we find different tools. The two most common for targeting GPUs are CUDA [14]

Listing 3: Vector Addition in expressed in CUDA

```
__global__ void addgpu(float *a, float *b, float *c) {
   int tid = blockIdx.x;
   c[tid] = a[tid] * b[tid];
}

void compute(float *a, float *b, float  *c) {
  // Allocate the memory on the GPU
  cudaMalloc((void **)&dev_a, N*sizeof(float));
  cudaMalloc((void **)&dev_b, N*sizeof(float));
  cudaMalloc((void **)&dev_c, N*sizeof(float));
  // Memory transfers: CPU to GPU
  cudaMemcpy(dev_a, a, N*sizeof(float),cudaMemcpyHostToDevice);
  cudaMemcpy(dev_b, b, N*sizeof(float),cudaMemcpyHostToDevice);
  // Launch CUDA Kernel into GPU
  addgpu<<< N, 1 >>>(dev_a, dev_b, dev_c);
  // Memory transfers: GPU to CPU
  cudaMemcpy(c, dev_c, N*sizeof(int), cudaMemcpyDeviceToHost);
}
```

and OpenCL [15]. What these models have in common is that there is a clear separation between the host code (the code that is executed on the main machine -such as a CPU- and the device code as the code that is executed on the target accelerator.

OpenCL is an standard supported by the Khronos Group that allows programmers to use any compatible heterogeneous hardware with the same source, such as CPUs, GPUs and FPGAs. CUDA is a tool created and supported by NVIDIA, and it only works with NVIDIA GPUs. An OpenCL program is composed of two main parts: the main host source code, that is statically compiled, as any other C/C++ program; and the device code, that is normally compiled at runtime by the driver implementation of the language itself (AMD driver, CUDA driver and Intel drivers are the main implementations for OpenCL).

In the case of CUDA, the source code is also split into two sections, the host code and the device code. Beginner CUDA programmers can use CUDA syntax. In this case, programmers need to compile with a separated compiler (`nvcc`) to obtain the binary. CUDA also provides a low-level API abstraction in which programmers explicitly provide a CUDA source and this is compiled and linked at runtime using the NVIDIA CUDA compilers in a similar way to OpenCL programs.

Listing 3 shows an example of a vector multiplication using the CUDA runtime API. The function `addgpu` corresponds to the CUDA kernel that is going to be executed on the GPU. Note that CUDA uses an explicit index that identifies the execution thread within the iteration space (there is no loop that traverses the array). This models radically differs from others such as directive-based, in which the developer simple annotates the sequential for-loops. The second function (`compute`) prepares the CUDA environment and launches the GPU kernel. It first allocates the data on the GPU (since NVIDIA GPUs and CPUs do not share memory), and then it performs the data transfers from the CPU to the GPU. Finally, it launches the kernel and performs the final copy back from the GPU to the CPU with the result of the computation.

On top of these two main programming models for GPUs, many researchers and industries have developed specific libraries that facilitate GPU programming. For example, TensorFlow [16] is a library, and a programming model, that uses NVIDIA GPUs and Tensor Cores for deep learning applications.

**Domain Specific Embedded Programming Models** CUDA and OpenCL are really complex programming models. Programs written in either OpenCL or CUDA need a good understanding not only about the programming model, but the underlying hardware architecture.

OpenCL and CUDA are programming models and parallel programming languages that target expert programmers that aim for optimizing the code at low-level. This increases complexity to read and maintain the code, and also, it makes it hard for non-expert to take advantage of the possible application acceleration by using this heterogeneous hardware.

To circumvent these challenges, there are many alternatives, and this is where research and innovations are currently focusing on. One example of these type of programming models is SYCL [17], in which programmers write a seamless C++ source code that some parts execute host and other device code. SYCL is an standard proposed by the Khronos

Listing 4: Kernel code-snippet to compute vector-addition expressed in SYCL

```
sycl::queue myQueue(gpuSelector);
myQueue.submit([&](sycl::handler *cgh) {
    auto a = d_a.get_access<sycl::access::mode::read>(cgh);
    auto b = d_b.get_access<sycl::access::mode::read>(cgh);
    auto r = d_r.get_access<sycl::access::mode::write>(cgh);
    cgh.parallel_for<class myKernel>(N, [=](sycl::id<1> idx) {
      r[idx] = a[idx] + b[idx];
    });
});
```

Listing 5: Vector Addition in expressed in Aparapi

```
public class Example extends Kernel {
  private float[] x, y, z;
  private float alpha;

  @Override
  public void run() {
    int idx = getGlobalId();
    z[idx] = alpha * x[idx] + y[idx];
  }
}
```

Group in that specifies an API and a subset of the C++ programming language to execute on heterogeneous systems. SYCL defines a subset of C++ to the target GPU, and that code is not distinguish from the rest of the C++ code. These type of programming models make much easier to develop, maintain and be understood, even by non-expert programmers.

Listing 4 shows the vector addition example implemented in SYCL. Any SYCL program is a C++ program with the extensions the data types and semantic that allow users to offload and execute code on any supported accelerator (e.g., a GPU). We show a sketch for the kernel computation expressed in SYCL. We first create a command queue using a GPU device (GPU selector). Then we submit a kernel to the command queue using a C++-11 lambda expression. In the lambda expression we need to obtain the type of **accessor** each variable will have within the compute kernel. In this case we set the input variables (`a` and `b`) as read-only. The result (expected in variable `d_r`) is set as write-only. Then, the kernel is expressed in a very similar way to OpenCL, with the addition of identifying the access of each variable between the host and the device, but using a C++-11 lambda expression.

In this category also we can find many other projects related to high-level programming languages such as Java, C#, R and Python. To name a few examples, Java Aparapi [18] offloads some Java special classes to the GPU using OpenCL; IBM J9 for Java-GPU computation [19] and Sumatra [20] (for computing Java streams into GPUs). Dandelion [21, 22] executes LINQ queries over the DotNet Virtual Machine on NVIDIA GPUs.

Listing 5 shows the same example of vector addition but implemented in Java-Aparapi. The method `run` is the one that Aparapi compiles to OpenCL for running on GPUs and CPUs. Notice also that the way of implementing the very similar to SYCL or OpenCL, in which the actual compute-kernel is expressed using OpenCL semantics through the intrinsics for indexing parallel loops, such as the `getGlobalId` in Line 7. Also, due to the fact that these programming models, such as SYCL and Aparapi, execute a subset of the input programming language, they break the semantincs of the underlying language.

**Programming Models for Reconfigurable Computing** The last category of programming models in heterogeneous computing is strongly related with the reconfigurable and programmable resources; also known also as FPGAs. This type of hardware devices offers flexibility, as the same device can be tailored to accelerate various application-specific tasks on-the-fly. Due to their ability to act as application-specific and programmable hardware resources, FPGAs use different programming models than CPUs and GPUs. There are mainly two types of programming models [23]: the Register-Transfer Level (RTL) and the High Level Synthesis (HLS). Figure 2 presents a high-level overview of both programming models, highlighting various key aspects in FPGA acceleration, such as the development time and the level of customization.

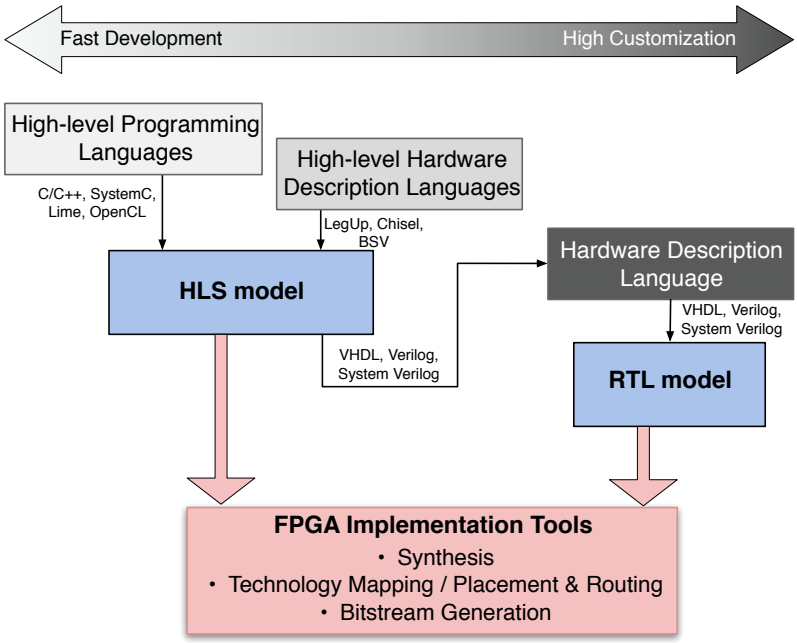


Figure 2: Programming Abstractions in Reconfigurable Computing.

The RTL model is a low-level abstraction of a digital circuit composed of two main parts; the registers (sequential logic) and the logic gates (combinational logic). In order to program a digital circuit in the RTL model, two hardware description languages (HDL) have been traditionally used, Verilog and VHDL. Both languages allow programmers to exploit low-level elements, such as registers and wires, which can be deployed in deep pipeline designs that can obtain higher performance compared against code emitted for CPUs and GPUs. However, programming via Verilog or VHDL requires high expertise and the development can be a time-consuming process depending on the complexity of the design.

Hence, the HLS programming model emerged to offer a higher level of abstraction than the RTL model, and subsequently make FPGAs more approachable to software programmers. The HLS model includes tools [24] that compile either high-level hardware programming languages, such as LegUp, Chisel, and Bluespec System Verilog (BSV), or high-programming languages (e.g., C/C++, System C, Lime.) into HDL code. The former set of tools exposes low-level customization primitives into the programmer level and achieves faster development time, as programmers can use a high-level hardware language rather than HDL code [25]. On the other hand, the latter set of tools includes frameworks that compile widely-used high-level languages into low level HDL. Following the HLS compilation process, the generated HDL code is passed as input to the vendor-specific FPGA implementation tools (e.g., Xilinx Vivado and Intel Quartus) which subsequently implement the executable binary code. The process of the binary implementation is usually split in three parts: a) the `synthesis`, which generates the netlist according to the HDL input; b) the `mapping-placement&routing`, which allocates the underlying resources and places on the device based on the specified design constraints (e.g., timing constraints); and c) the `bitstream generation`, which compress the implemented hardware design from the previous step into an executable binary file.

Furthermore, two of the most dominant FPGA vendors, such as Intel and Xilinx, have recently introduced OpenCL support for FPGAs, thereby indicating it as a cross-platform compatible programming model. However, although programming with OpenCL can be portable across multiple heterogeneous devices, the performance is not portable yet because of the diversity in device characteristics.

**Summary of Challenges of Parallel Programming Models** Programmability of heterogeneous systems is one of the main challenges. Due to the end of the Moore's Law, industry and academia implement and create custom hardware in order to scale and specialize computing systems that better use energy and offer high-performance. The main trade-off is that new custom hardware normally require new programming models to achieve high-performance. The next Section we will describe the new trends in academia and industry that addresses these challenges.

To summarise, programmability of heterogeneous systems is one of the main challenges. Due to the end of the Moore's Law, industry and academia implement and create custom hardware in order to scale and specialize computing systems

that better use energy and offer high-performance. The main trade-off is that new custom hardware normally require new programming models to achieve high-performance. Section 3.2 will describe the new trends in academia and industry that addresses these challenges.

### 2.4 Resource management

The scale of heterogeneous computing systems has been rapidly growing and as of today they contain computing and storage devices in the range of tens to hundreds of thousands, e.g. in date centres, hosting complex applications and relevant data. Consequently, effective resource management and scheduling policies need to be put in place to achieve high scalability and operational efficiency. However, these policies face challenges with the provision of costly mixed CPU, GPU and FPGA types, and high-performance low-latency interconnects.

In the domain of cloud computing, there are several frameworks for the orchestration, scheduling, and deployment of CPU clusters, such as YARN [26] and Kubernetes [27]. The lack of specialized resource managers and orchestrator for FPGAs has limited the deployment and wide utilization FPGA-based heterogeneous clusters. Major cloud and High Performance Computing (HPC) providers such as Amazon, Azure, Alibaba, Huawei, and Nimbix have started deploying FPGAs in their data centers. However, the development tools and frameworks offered by FPGA vendors and cloud providers do not allow the utilization of FPGA cluster from multiple applications. In case a user wants to deploy several FPGAs (either on the same server or on multiple servers), the user will have to configure the FPGAs, distribute the data manually and to collect back the results from each device; a tedious and error-prone process. Additionally, if multiple users or applications/threads wanted to have access to the resources of an FPGA cluster, a serialization mechanism is required that will make sure that there will be no conflicts and the requests to the FPGA resources will be made in a proper way.

Therefore, an efficient resource manager for heterogeneous computing is still a challenge and it is required in order to allow the easy deployment, scaling, management and utilization of hardware accelerators.

### 2.5 Quality of Service

With applications turning to heterogeneous computing to offload workloads and scale to their growing requirements e.g. on execution delay, Quality of Service (QoS) provision from the perspective of the heterogeneous computing environment, e.g. architecture, resource utilisation and management, energy consumption, becomes paramount [28].

QoS provision is associated with a number of challenges with respect to application development, deployment and operation in heterogeneous computing environments: 1) resources (computing, data, and networking) abstraction to advance software application development, e.g. how to abstract data beyond simple semantic annotations that are expressive and carrying out additional information about execution requirements, network topologies and data sources; 2) exploitation the potential of (distributed) heterogeneous infrastructures, e.g. how to build applications that exploit the distributed infrastructure in a transparent way, and 3) (De)composition and transformation of all aspects in relation to non-functional properties and conversion to different target infrastructures, e.g. how to compose applications from software components to support the required functional and non-functional requirements and map these onto the distributed infrastructure.

Such QoS provision in various configurations and situations is complex. Effective methods and tools are needed should configure the underlying infrastructure to meet the required QoS to compose and package application software components, to (possibly) configure the virtualisation layer and deploy them on allocated hardware resources for achieving application quality requirements. These methods and tools will rely on a middleware capable of monitoring ongoing execution of multiple applications. It is therefore important that the application's software is in a malleable form so that its execution can be adapted at runtime to maintain the quality trade-off among all operating applications.

### 2.6 Predictability

Another important area that involves efficient scheduling, heterogeneous hardware management, live task migration, and security, to name a few, is predictability. The goal is to anticipate what are the resources needed or future events in order to make informed decision on their allocation, improve their utilization as well as guarantee the safety of applications running on heterogeneous hardware. This is, in fact, a hard problem, which has attracted the interest of many researchers, who often turn to machine learning strategies to facilitate such prediction [29, 30, 31].

For a wide class of Cyber-Physical Systems (CPS) and IoT applications, the ability to reason on their behaviour, and provide guarantees on their correct response, surpasses their functional needs and includes the requirement of temporal correction (safe and secure execution includes the time dimension). Predictability may impact performance (guaranteed

performance needs different, less throughput based, approaches), or energy. At the same time, with the increasing shift to complex parallel architectures, it will be difficult, if not impossible, to provide efficient predictability.

System design must consider how to build a predictable system with HW/SW components whose timing behavior is provably analyzable only in isolation, but not in a platform that integrates hundred-to-thousands of them. The reason is that, traditional approaches and frameworks to timing analysis are over-pessimistic (or, completely fail) when dealing with the inherent architectural complexity of modern heterogeneous architecture, making them in fact inapplicable to modern industrial settings, where predictability (which in turn, means safety and certifiably) and peek performance must coexist at low power and size envelope. Researchers proved that, especially, the contention to access shared resources, greatly affects average- and worst-case performance. For instance, authors in [32] showed how contention on shared memory and caches can harness performance by a factor ox 8-10 $\times$, when not adequately mitigated. Another approach to tackle such issue is the adoption of software-based techniques to partition the hardware resources both in space and time to the requesting cores and (in turn) OS threads.

### 2.7 Sustainability

Heterogeneous computing systems' "power" challenges have shifted from mainly being addressed at the devices and circuits level, to their current position as first-order constraints for architects and software developers. Moreover, power consumption is a limiting factor due to physics with the end of the Moore's Law era and the ever increasing cost of energy [28]. With power concerns creeping up the implementation layers, while application-level changes alter the nature of computation being performed, the natural approaches and opportunities for power mitigation require constant innovation [33].

Moreover, the biggest challenges to application performance lie with not only efficient node-level execution on heterogeneous hardware but power consumption as well. CPS and IoT fields are discovering new applications where relatively high performance is required from systems which by the nature of the domain are physically constrained, by size, weight or energy dissipation, or by the reliance on battery or solar energy. Examples include vehicles where space, weight, heat dissipation and reliance on the engine for power are all constraints. Another aspect is data processing.

While exploiting the full potential of the next generations of computing systems based on heterogeneous parallel architectures, it is also essential to promote not only their physical and economic viability but energy efficiency awareness among all their stakeholders [34]. Application developers need to fully understand the nuances of different hardware configurations and software systems, as well as consider additional difficulties in relation to performance, mixed-criticality and power consumption resulting from heterogeneous systems. One of the important steps in software design for low power, above all other power optimisations, is software correctly fitted to the capabilities of the underlying hardware to support high-performance and energy efficiency.

### 2.8 Security

Nowadays, security features in processors have become the norm. Numerous examples include the SPARC T4 [35] and the Intel Advanced Encryption Standard New Instructions (AES-NI), an encryption instruction set that accelerates the encryption of data in the Intel Xeon and Core processor families [36]. Other approaches for processors' security are based on the concept of obfuscation [37, 38]. For example, Control Flow Integrity (CFI) [39, 40, 41, 42] is a mechanism that aims to circumvent code injection attacks by monitoring the control flow instructions (branches), and rejecting them in case they do not meet the correct execution flow. A second example of obfuscation to prevent code injection attacks is Instruction Set Randomization (ISR) [43, 44, 45, 46, 47], which creates and assigns a unique randomized instruction set to each running process. The creation of this new instruction set is based on XOR-ing the original instructions with a hash key. As a result, there is no exposure of any meaningful code to attackers, unless they determine that key.

Although, the aforementioned techniques have low implementation cost in hardware, in practice they harden users' experience. For instance, software updates provided by third party software have to be obfuscated; and shared libraries cannot be reused, due to the per-application code randomization basis. Apart from protected code execution, security has been expanded also to facilitate secure boot and access to particular data zones. This concept has been employed by hardware vendors (e.g. Intel's Software Guard Extensions (SGX) [48], Arm's TrustZone [49]) to isolate the execution environment into two groups (a secure one and an insecure one). The secure environment can be used to store sensitive information such as sealed keys that are used for encrypted operations, while the insecure environment can be used to execute any third-party application that does not interact with private data.

Finally, the hardware approaches are mainly focusing on securing the execution on the main processors. Although, there are examples of accelerators (e.g., FPGAs) that have been used as co-processors for cryptography [50], the lack of

systematic and secure-by-design execution across diverse accelerators, such as GPUs, FPGAs, TPUs, is vital. Therefore, security in the context of heterogeneous architectures will be a first-order challenge in the near future.

### 2.9 Networking and Interconnects

Technologies such as Software Defined Networks (SDN) and Network Function Virtualisation (NFV) intend to build agile, flexible, and programmable networks to reduce both capital and operational expenditure to support heterogeneous hardware environments. General purpose processors are not optimal for a number of computation tasks, including communication. This results in lower performance (throughput and latency) and increased (but needless) processor utilization. Modern systems offload the communication tasks to special hardware. FPGA-based accelerators can be used to implement and evaluate experimental network protocols for HPC and data enter systems. As with most new accelerator, implementing high performance networking gear in FPGAs and evaluating with real applications is a complex task with high startup overhead. The hardware has to thoroughly thought, simulated, evaluated, implemented in hardware, coupled with systems-software, debugged, and evaluated once more running real applications.

MPSoCs that couple low-power ARM processors in the same package with programmable FPGA logic are currently available. These platforms allow us to implement and experiment with new solutions that tightly couple the network interface with the processor. This approach is used in [51] in order to design and test next-generation network adapters with advanced reliability features and improved latencies. For instance, by re-using the ARM System Memory-Management-Unit (SMMU) to translate virtual to physical address, using the per-process page tables that reside in DRAM, one can bypass the need to pin the communication buffers, thus reducing the communication latency, and implifying the programming model, and reducing the area footprint of the network interface. Performing the reliability functions inside the network adapters (timeouts, positive and negative acknowledgements, and end-to-end re-transmissions), one can fully bypass the TCP/IP stack.

To support heterogeneous platforms, one current challenge is to design interconnects that unify traditional IP and memory-semantics, e.g. Remote Direct Memory Access (RDMA) networks, as well as accelerator traffic. FPGAs again offer a unique vehicle to study such new deployments, that fully avoid the need for OS intervention and offload the main processor in the data path.

## 3 Emerging Trends and Impact Areas

As heterogeneous computing and relevant research matured over the years, it led to substantial advances in the underlying technologies such as real-time heterogeneous platforms. In addition to these, other emerging trends in ICT such as the Internet of Things, machine and deep learning, and big data also have started influencing heterogeneous computing research and have offered wide opportunities to deal with the open issues in the underlying challenges. Some of the emerging trends and impact areas relevant to heterogeneous computing are discussed next.

### 3.1 Emerging FPGA-based Heterogeneous Architectures

Although there are numerous heterogeneous and emerging computing architectures, this section focuses on a specific expanding and very promising set, those employing FPGAs. There is an emerging trend to attach customized hardware, and, in particularly, FPGAs in current computing systems, such as in data centers and HPC systems, which this section will present in the context of the ECOSCALE project (http://www.ecoscale.eu/) through the Unified Logic (UNILOGIC) architecture [52].

Escobar et al. [53] present a thorough survey on algorithms implementation in heterogeneous HPC infrastructures that integrate diverse resources, including CPUs, GPUs and FPGAs, and provide guidelines for effectively employing FPGAs in HPC. In this survey, it has been estimated that half of the lifetime cost of HPC platforms is devoted to electrical power. An additional remark of this work is that high level synthesis tools such as Vivado HLS (by Xilinx) and Catapult C (by Mentor Graphics) have emerged in order to overcome the programmability overhead when designing FPGA-based architectures. It is also noted that a basic part of the success of CPUs and GPUs, in the HPC domain, is due to the widespread support of libraries, unlike current customized FPGA-based solutions. Similar research work in literature [54, 55, 56, 57, 58, 59, 60] has focused on showcasing increased performance on reconfigurable systems, especially when comparing the performance per watt of the FPGAs against the respective of the CPU and GPU counterparts. Moreover, these works also emphasized on the overhead in programmability when hardware designers build FPGA accelerators via common FPGA design tools.

One challenge remains: how to improve the programmability of multi-FPGA environments within HPC infrastructures, while providing a low latency communication architecture, scalable to a very large volume of interconnected FPGAs.

In order to address this, ECOSCALE has developed UNILOGIC, a HPC-tailored parallel architecture and firmware that efficiently incorporates multiple FPGAs [52]. The architecture employs the Partitioned Global Address Space (PGAS) model and extends it so as to include hardware accelerators, i.e. tasks implemented in the reconfigurable resources of the FPGAs. The main advantages of UNILOGIC are : a) the hardware accelerators can be accessed directly by any processor in the system, and b) the hardware accelerators can access any memory in the system. In this way, the proposed architecture offers a unified environment where all the reconfigurable resources can be seamlessly used by any processor/operating system. Moreover, UNILOGIC provides hardware virtualization of the reconfigurable logic so that the hardware accelerators can be shared by several applications or tasks so as to be able to act in par with the multi-processor systems The UNILOGIC architecture can also be extended to support novel security and privacy mechanisms of the shared resources.

Within each reconfigurable device the resources are separated into *i)* a static partition, which provides the PGAS-related communication infrastructure, and *ii)* fixed-size and dynamically reconfigurable slots that can be programmed and accessed independently or combined together so as to support both fine and coarse grain reconfiguration; the latter has been achieved by utilizing the partial runtime reconfiguration feature of today's FPGAs so as to dynamically reconfigure the slots in real time.

The UNILOGIC architecture partitions the system design into several processing nodes, called Workers, which communicate through a hierarchical communication infrastructure or mesh-like topology. Each Worker comprises of conventional processing units, memory, reconfigurable logic, and accelerator controllers that provide access to the reconfigurable resources in order to program and execute accelerated tasks in hardware at runtime (Figure 3).

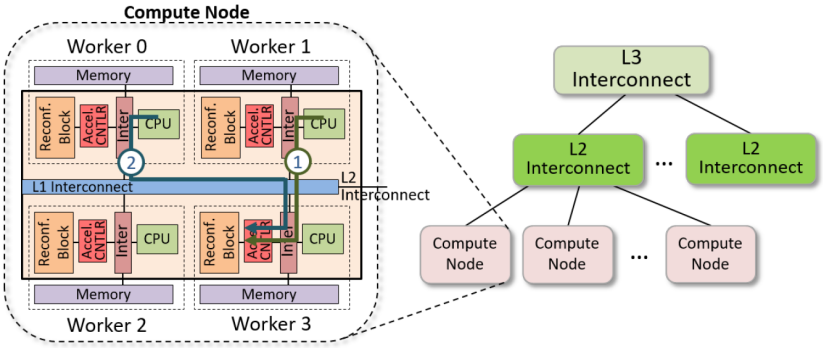


Figure 3: The UNILOGIC architecture

The UNILOGIC architecture has been evaluated on a custom prototype that consists of two 1U chassis. Each chassis includes eight interconnected daughter boards, called Quad-FPGA Daughter Boards (QFDBs), and each QFDB supports four tightly coupled Xilinx Zynq Ultrascale+ MPSoCs as well as 64 Gigabytes of DDR4 memory. Thus, the prototype features 64 Zynq MPSoCs and 1 Terabyte of memory in total. UNILOGIC has been tuned and evaluated on this prototype using both low-level performance benchmarks as well as two popular HPC real-world applications, one compute-intensive and one communication-intensive. Based on the measured results, UNILOGIC offers impressive performance that ranges from being 2.5 to 400 times faster and 46 to 300 times more energy efficient compared to conventional parallel systems utilizing only high-end CPUs.

### 3.2 Emerging Heterogeneous Programming Models

This paper has shown that currently there is no single computer architecture to better execute all types of workloads efficiently. Due to increasing demand of compute and variety of workloads, such as big data processing, machine/deep learning, cryptocurrency, IoT, security and block-chain technologies, companies and researchers are investigating and providing new computer architectures that execute those workloads in a more efficiently. For instance, Google has develop and built a new processor for running TensorFlow in a more efficient manner, called Tensor Flow Processing Units (TPUs) that are currently shipped on last generations of NVIDIA GPUs. Another case is the Wafer-Scale Engine (WSE) developed by Cerebras as a new hardware specialized for accelerating deep-learning that contains 400k AI cores.

As we introduced in the Section 2.3, there are many programming models and approaches to develop applications for heterogeneous systems. However, those approaches are often limited to the mainstream programming languages that are underneath, which lack of ways of expressing parallelism, and they are also considered low-level for many potential users of the new heterogeneous hardware. One thing to notice is that many of the standards and programming models

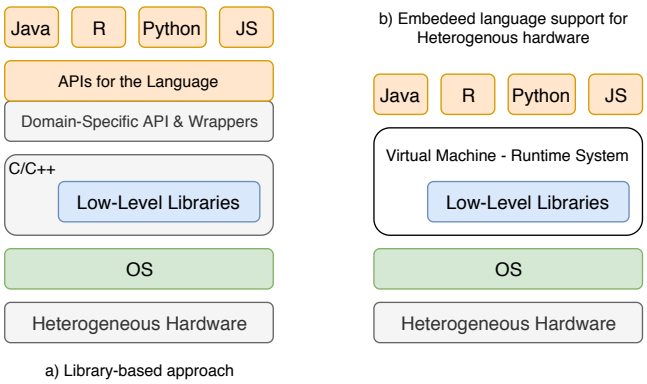


Figure 4: Software stack for running applications implemented in managed programming languages for two different approaches. The approach a) shows how currently high-level programming languages can make use of heterogeneous hardware via native APIs. The approach b) shows a different strategy in which the underlying runtime and virtual machine, that abstract the program from the hardware details, can automatically make use of the heterogeneous hardware.

have been created on top of low-level programming languages, and, in particular, on top of the C/C++ programming models. However, not all programmers use C/C++ and Fortran programming languages.

**Time for higher abstractions and managed programming languages** By carefully studying the trends over the past years of the most common programming languages that are currently used by industry and academia, such as the TIOBE index [61, 62], we see that more than 5 out of the top 10 programming languages are interpreted and/or dynamically typed programming languages, such as Java, C#, Ruby, Python, R and JavaScript. Additionally, we see that, in the big data application-domain, the most used programming languages are Java, Scala, Python and R.

*Now the question is how these programming languages make use of accelerators such as FPGAs and GPUs.* Figure 4 shows the typical hardware/software stack for programming heterogeneous architectures from high-level languages such as Java, R, Python or JavaScript.

As Figure 4-a shows the current trend to provide external libraries that make calls to native code. Hardware vendors normally provide an Application Programming Interface (API), or a domain-specific API to interact with the low-level hardware from managed programming languages. The implementation of those libraries are normally written in system's languages such as C and C++, that dispatch the native calls to the actual heterogeneous hardware. The native code either provides pre-compiled kernels, or exposes an API to bypass kernels from high-level languages to low-level such as OpenCL, CUDA or Verilog. The main problems with this approach is that developers need to know low-level hardware details in order to make use of these new hardware, because the API exposes hardware details, or because programmers are tied to a specific set of calls to solve concrete problems. However, this is not the purpose of high-level and interpreted programming languages, in which the code is written one, and there is a runtime system (aka the Java Virtual Machine) that automatically executes and manages the memory of the input program without the need of the developer's intervention. Figure 4-b shows an alternative approach in which high-level programming languages make use of an existing language runtime-system, or a Virtual Machine (VM), that knows how to automatically generate and execute code on heterogeneous hardware. Although promising, this last approach is mainly under research, with only a few exceptions that are available for mainstream commercial use, such as AMD Aparapi [18], or IBM-GPU J9 [19]. Let's now discuss in more details each of the approaches.

**Programming via external libraries and domain-specific APIs** Following the approach illustrated in Figure 4-a, one of the most popular set of libraries is for machine learning and deep learning algorithms. Perhaps, the most common library for machine learning and image classification nowadays is TensorFlow [63], a Google programming framework for deep learning which is currently available for Python, Java, C and Go programming languages. In addition to TensorFlow, there are other libraries and frameworks such as PyTorch [64] for machine learning and image classification. What these type of frameworks have in common is that they target a specific set of applications, e.g., deep learning, computer vision. They facilitate programming to developers by exposing a clean API and their implementations are highly optimized to use the latest and most advanced hardware, such as Tensor Processing Units (TPUs) for TensorFlow computation. However, if developers want to extend that functionality, they have to either implement the missing functions in those libraries, or wait for the library provider to include them. Another drawback for providing specific

Listing 6: Vector Addition expressed in TornadoVM

```
public class Compute {
  public static void vertorAdd(float[] a, float[] b, float[] c) {
    for (@Parallel int i = 0; i < c.length; i++) {
        c[i] = a[i] + b[i];
    }
  }
  public static void run(float[] a, float[] b, float[] c) {
    new TaskSchedule("s0")
       .streamIn(a, b)
       .task("t0", Compute::vectorAdd, a, b, c)
       .streamOut(c)
       .execute();
    }
}
```

and optimized libraries is that, if hardware changes, the library provider have to rewrite, most likely, many portions of the code base to adapt it to the new hardware (e.g., a new GPU model, an FPGA, or a new custom designed accelerator).

There are other APIs, called native-wrappers, that directly expose and leverages the low-level programming models of the heterogeneous hardware, such as the GPU programming for OpenCL or CUDA, into the high-level programming languages. There are many wrappers for OpenCL programming over Java, C#, Python, R, etc. However, with this approach, programmers need to deal with at least two different programming models and execution models, the base language itself (e.g., Java) and the heterogeneous programming model (e.g., CUDA). This has implications in productivity and portability of these high-level applications, because some parts of the programs are tied to specific hardware requirements. However, this is not the purpose of using hardware agnostic, interpreted and dynamic programming languages. An alternative approach is to automatically use the heterogeneous hardware by using a specialized Virtual Machine that performs the code compilation and transparent execution of applications written in high-level programming languages into heterogeneous hardware.

**Emerging Heterogeneous Runtime-Systems** Another trend (mainly in research) is to automatically compile and execute code from existing mainstream programming languages, such as Java, Ruby and R, into high-efficient GPU and FPGA code without the need of any external library. Those new compilers and runtime-systems are mainly under research. One example is TornadoVM [65, 66], which provides an abstraction of the execution on any heterogeneous device to execute Java programs on GPUs, CPUs and FPGAs without changing the existing Java code. TornadoVM is defined as a plugin to OpenJDK that allows programmers to automatically execute Java, R, Python, Node.js and Ruby programs on heterogeneous hardware, without any low-level knowledge about the actual hardware. Furthermore, TornadoVM can dynamically migrate execution from one device to another at run-time based on profiling information.

Listing 6 shows a full example of vector-addition computation expressed in TornadoVM. TornadoVM receives as input legal Java code, and it provides an API to identify the methods to be executed on heterogeneous devices, such as a GPU or an FPGA. The Tornado runtime system will compile these methods into OpenCL C code, and it will execute the generated target binary/bitstream into the corresponding device. All of this is performed without any knowledge from the users' perspective about hardware heterogeneity. Additionally, this code is scheduled by the Tornado runtime-system and can be executed in any OpenCL compatible device, including GPUs, FPGAs, and multi-core systems.

Similar work have been done by AMD such as Aparapi [18] and Sumatra [20], or by Microsoft Research, such as Dandelion [21]. Recently, IBM has introduced a GPU-compiler for Java programs to be executed on NVIDIA GPUs, called IBM J9 [19]. IBM J8, as well as Sumatra, accelerates some operators from the Java 8 Stream API into GPUs by offloading Java lambda expressions into NVIDIA GPUs. Marawacc-compiler and runtime [67, 68] is a similar approach to TornadoVM, which compiles Java, R and Ruby code to OpenCL to execute workloads on multi-core CPUs and multiple-GPUs via OpenCL.

Similarly, ALPyNA [69, 70] is a Python compiler and a runtime system that automatically parallelize loops into CUDA kernels to run on NVIDIA GPUs. Along the line of AlPYNA, MEGAGUARDs [71] performs auto-parallelization of whole loop-regions in Python and generates OpenCL C code. In that way, MEGAGUARDs can accelerate Python code by automatically using GPUs and multi-core systems.

All of these type of approaches are classified as Domain Specific Embedded (DSE) programming models, in which the user provides a single source code, and the compiler offloads and executes some parts to the corresponding accelerator. DSE approach is a promising research direction with the aim to facilitate parallel and heterogeneous programming and make heterogeneous hardware more accessible to a wide set of developers, programmers, researchers, not necessary software developers but also biologist or physiologist, to name a few.

### 3.3 Virtualisation

The application of virtualisation in heterogeneous computing is showing clear benefits with its multiple properties and can potentially be supported thanks to Virtual Machines (VMs) and the use of containers technology, in order to provide efficient resource sharing and system security. Network Function Virtualization (NFV) also shows great potential in the future of network security and stability. Moreover, low-level hardware virtualisation technologies, such as I/O virtualisation and Inter-Process Communication virtualisation, have provided energy-efficient approaches. Virtualisation hides much of how the system works in view of global optimization.

Machine learning applications benefits immensely from accelerator technologies, especially from GPUs, since they require substantial processing that can be executed in parallel. Tensorflow [16] is a framework used to develop and run these machine learning algorithms, and can issue kernels on the accelerators. One problem with such framework is that it requires exclusive access to the accelerator, thus does not foster accelerator sharing across different applications.

Thus, Virtualisation of accelerators in hardware is attracting attention, e.g. FPGA-based acceleration [52]. Such approach encompasses a Scheduler-Mailbox block pair and supports ease of programmability. This involves automating the distribution and dividing of big tasks into smaller ones, which can be executed by the reconfigurable hardware accelerators, while being transparent at the application level. Such a goal pertains to a virtualisation infrastructure which aims to virtualise the acceleration resources of a single FPGA, and then at System-level, upscale by similarly operating on a multi-FPGA unified environment. Hence, the hardware accelerator controller can be connected to, and thus control, a varying number of hardware accelerators.

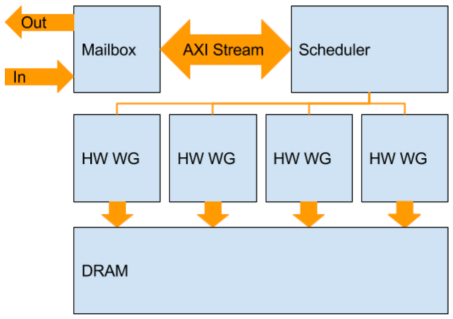


Figure 5: Overview of the virtualization block and its interfaces.

This functionality is depicted in Figure 5, where accelerators are designated as Hardware Work Groups (WG). The Mailbox on top incorporates two FIFOs for write and read operations. Acceleration request commands are first issued to the mailbox (to be then propagated to the Scheduler) by writing to the incoming FIFO. Any required status information can be read from the mailbox's outgoing FIFO, as the Scheduler responds with messages through the mailbox. These messages notify the initiator application for configuration completion, work completion, as well as various errors that may occur, such as wrong opcodes.

Another approach is to provide temporal and spatial sharing of accelerators, i.e. applications can be executed in parallel on an accelerator such as FPGAs and GPUs (spatial sharing), or can be time multiplexed, under different programming models, i.e. CUDA, OpenCL [72]. Vinetalk [73], [72] is a runtime system that implements such approach and allows different applications to run natively in VMs and containers.

NVIDIA provides Multi-Process Service (MPS) with which applications can share (temporally and spatially) an NVIDIA GPU. MPS supports only First-Come-First-Served (FCFS) scheduling, consequently it cannot be used when SLA guarantees are desired. On the contrary, Vinetalk manages accelerator memory and supports arbitrary scheduling policies that can for instance prioritise high priority kernels over low priority ones. Additionally, Vinetalk, in contrast with MPS, can take advantage of multiple accelerators that exist in one node and schedule applications according to their requirements.

Transparent GPU virtualization is also made available in offloading platforms such as GVirtuS [74] which enables Android devices with little or no GPU support to run NVIDIA CUDA kernels by transparently migrating their execution to high-end GPGPU servers. The GVirtuS platform is highly modular, and exposes a rich Application Programming Interface (API) to developers, making it highly versatile while hiding the complexity of the underlying network layer.

### 3.4 Quality of Service Support

Nowadays applications become more compute intensive. For instance, machine learning and deep learning algorithms are compute intensive, since matrix multiplications dominate [75]. In addition, to these demands for increased compute capacity has been the requirement for low latency responses. Pattern matching and recommendation algorithms need to respond to the end-user with low and bounded latency, in the range of milliseconds (Service Level Agreement-SLA [76]). One solution to serve this increase in computational needs is to scale out using only general purpose CPUs. However, such approaches increase energy consumption. The challenge, therefore, is to increase processing capacity under the same power budget of commodity CPU servers.

A response to these workload trends and technology limitations has been the use of accelerators such as, GPUs, FPGAs, and TPUs in data-centers. Accelerators consist of multiple thin cores, hence they can provide high throughput due to massive parallelism, at a lower power budget. Although resources in cloud environments are typically shared, most cloud providers offer accelerators in a dedicated manner due to technological limitations, as the lack of preemption support. This exclusive assignment improves Quality of Service (QoS) of applications at the cost of accelerator utilization, because a single task or application is not typically capable to fully utilize an accelerator [77].

Previous work [78, 79, 80] has worked towards increasing mostly GPU utilization by sharing GPUs across user-facing and batch processing tasks [78]. User-facing tasks require tail latency guarantees based on their SLA [76]. The execution time of user-facing tasks, such as the inference in machine learning models, ranges from several microseconds up to a few hundreds of milliseconds. In contrast, batch applications do not have strict response-time requirements per task and are latency tolerant [81]. To ensure SLAs of user-facing tasks previous work has adopted SLA-oriented scheduling policies [78].

Existing SLA-oriented scheduling policies for GPUs [78, 79] ensure that more than 95% of user-facing tasks meet their SLA. However, these studies only consider *batch tasks with execution times similar to the SLA*. Under this assumption, one can afford to wait for a running batch task to finish before launching new user-facing tasks. However, batch tasks can have execution time orders of magnitude longer than user-facing tasks [80]. Current SLA-oriented approaches cannot provide QoS to user-facing tasks, when sharing a GPU with long running batch tasks.

Already existing approaches have addressed the problem of long running batch tasks using *GPU preemption*. With GPU preemption, the currently executing task is stopped and its state is stored either (1) in the GPU or (2) in the host memory. However, there are no approaches that are able to preempt tasks running to other accelerator types, as FPGAs, TPUs.

### 3.5 Self-Adaptative Systems

In Section 2.2 the increasing prevalence of Non-Von Neumann computer architectures was discussed, including the use of FPGAs and many-core GPGPUs. The variety of accelerators has led to the requirement for programming models to transform code from high level languages to the underlying heterogeneous architecture. The challenge is further increased by having to adapt the system to changes at both application deployment and runtime such as the availability of accelerators which may require techniques such as dynamic compilation of code to make use of the available resources as discussed in section 3.2. It may also require ensuring that there are multiple different versions of the same application available [82, 83] in order to take advantage of hardware acceleration when it is available. An accelerator's availability may relate to competing workloads all vying for time on the available accelerators. This gives rise to research questions relating to the handling of the different deployment options for mapping workloads and different implementations of the same application onto the underlying hardware. In particular this requires the discovery of the affinity of a particular application to a given accelerator and the likely benefit it is to obtain. Managing the trade-offs between competing applications whilst considering an applications affinity to an accelerators is no trivial task.

Overall the increased complexity from hardware heterogeneity gives interesting challenges in regards to a more global optimisation of such a complex environment. This optimisation may include aspects such as energy efficiency, performance, data movement, cost, time-criticality, security and dependability [34]. Heterogeneity not only adds complexity but may introduce constraints in itself. Computation at the edge induces new constraints in terms of available power, energy and performance while still requiring aspects such as fault tolerance and Quality of Service (QoS). Managing these constraints and in general overall system performance requires monitoring and actuators to control and balance both global system requirements as well as those of the individual users.

The trade-offs and adaptation made requires guidance and understanding of the possible impact of any changes made. This implies the need for monitoring, modelling and potentially learning behaviour. Power models for example can improve upon instruction level power estimation at the system-level [84] which in turn provides guidance on the most appropriate form of adaptation to take. Individual models can be integrated to form a more holistic view of the overall

system and manage the competing aspects of the overall systems optimisation. The scale and type of modelling that is utilised may depend upon the overall scale and complexity of the system as well as the perceived benefits it offers, relative to the overhead caused by all aspects of adaptation (i.e. monitoring, modelling, decision making, and actuating). Adaptation mechanisms themselves have overhead that must be considered. For example adaptations may require hardware changes such as the reconfiguration of FPGAs in order to manage the different workloads that are applied. Work towards making these reconfiguration as seamless as possible [85] increases the applicability of the forms of adaptation available to the system as a whole. Overall the balancing between total knowledge of the system, the systems distributed nature, the optimality of any deployment plan and the overhead of generating and executing adaptation needs careful consideration. The "Self-*" approach may allow the reconfiguration of systems in a broader system and ensure minimum mode of operation even in degraded situations. In the literature, different approaches for Self-Adaptive Systems construction can be found and categorised. These can be linked to dimensions such as adaptation control (decision criteria), time (reactive versus proactive), level (application, system software, communication) as well as MAPE (Monitor, Analyse, Plan and Execute) activities. Current trends for engineering systems include the use of control theory, nature-inspired and machine learning approaches [86].

### 3.6 Real-Time Heterogeneous Platforms

Autonomous systems, such as self-driving cars and drones are the hottest application domain for state-of-the-art Real-Time systems, and they are currently driving advanced research in the field. The next-generation of partially and fully autonomous cars will be powered by embedded many-core platforms. Technologies for Advanced Driver Assistance Systems (ADAS) need to process an unprecedented amount of data within tight power budgets, making those platform the ideal candidate architecture.

Integrating tens-to-hundreds of computing elements that run at lower frequencies allows obtaining impressive performance capabilities at a reduced power consumption, that meets the size, weight and power (SWaP) budget of automotive systems. Especially, integrated GPGPUs (iGPUs)[87, 88, 89] are today's preferred to other acceleration paradigms, e.g., based on FPGAs or application-specific integrated circuits (ASICs), in applications with data-parallel workloads, such as computer vision and AI systems employing deep neural networks. This is the case of advanced automotive systems, where AI/DNN are increasingly being adopted as reference for building partly- or fully- automated vehicles of tomorrow. Unfortunately, these systems demand not only for high peek performance, but also –and especially– worst case performance, and the increased architectural complexity of modern iGPUs makes it extremely cumbersome to perform an effective non-pessimistic worst-case timing analysis of system. Having impressive average performances with no guaranteed bounds on the response times of the critical computing activities is of little if no use in safety-critical applications.

### 3.7 Timing predictability *via* resource management

Timing predictability is the capability of a system to provide a response in defined amount of time, in the worst case. This property is especially amenable in Real-Time (RT) systems, which is where the research on timing predictability is pushed to the maximum, and where the state-of-the-art solutions are adopted. For this reason, in this section we will refer to Real-Time systems, without loss of generality. RT systems are roughly split in three macro-categories, namely, *hard RT*, *firm RT* and *soft RT*, depending how much timing predictability affects system functionality. In the former case, it is treated as a failure which might even harm human lives (es. avionics systems), while the other cases, the QoS degradation might affect system functionality in a less severe manner.

In Real-Time systems, applications are modeled by a set of *tasks*, that repeatedly span over time, in a *periodic* or *sporadic* manner. Each RT-task is characterized by a *Period* and a time *Deadline* at which the RT-task must be accomplished, to ensure the integrity of the ovDjemameerall systems. To enable robust and *certifiable* systems, in "traditional" RT theory, an accurate modeling of such tasks is carried on with a so-called *worst-case timing analysis*, and the resulting timing behaviors of the RT-tasks is composed using well-known frameworks, to provide an optimal mapping of tasks to available computing engines (CPU cores): this is called the *scheduling* theory.

When heterogeneous architectures made of complex many-cores come into play, it is clear how *cores are not anymore the scarce resource in the system, hence the resource that should be scheduled*. Hence, today's researchers agreed that shared components, such as memory banks, I/O devices, etc play the key role in this respect [90], [91], [92].

A first solution to this problem is to devise new architectures, or a *provably certifiable* subset of hardware blocks in existing computing platforms, so that a so-called *safety domain* can be used in this specialized application domain. Several hardware providers followed this approach: the most relevant examples are probably top-class platforms from Xilinx, such as the Ultrascale+ and Versal embedded accelerators. However, this (yet appealing) approach has two drawbacks. First, by reducing the subset of components that are actually used by an application, in fact we **underutilize**

the platform, causing a waste of resources. Secondly, unfortunately, the aggressive time-to-market strategies of hardware providers (NVIDIA *uber alles*) makes it impossible to stick to a given platform. For instance, the production-grade, ASIL-compliant NVIDIA Drive PX board, has been soon discontinued in favour of the new, more powerful Pegasus device. This tremendously complicates the work of, e.g., automotive and avionics engineers, that inherently require long-living HW and SW components software updates and support.

A second approach is to devise generic methodologies, implemented at the middle layers of the technological stack, to partition in space and time an existing hardware. Figure 6 shows how this was implemented in the Hercules H2020 project [93]. As Figure 6 shows, it employs a mix of Operating Systems, Hypervisor and custom/proprietary drivers that work synergistically to provide the maximum degree of predictability.

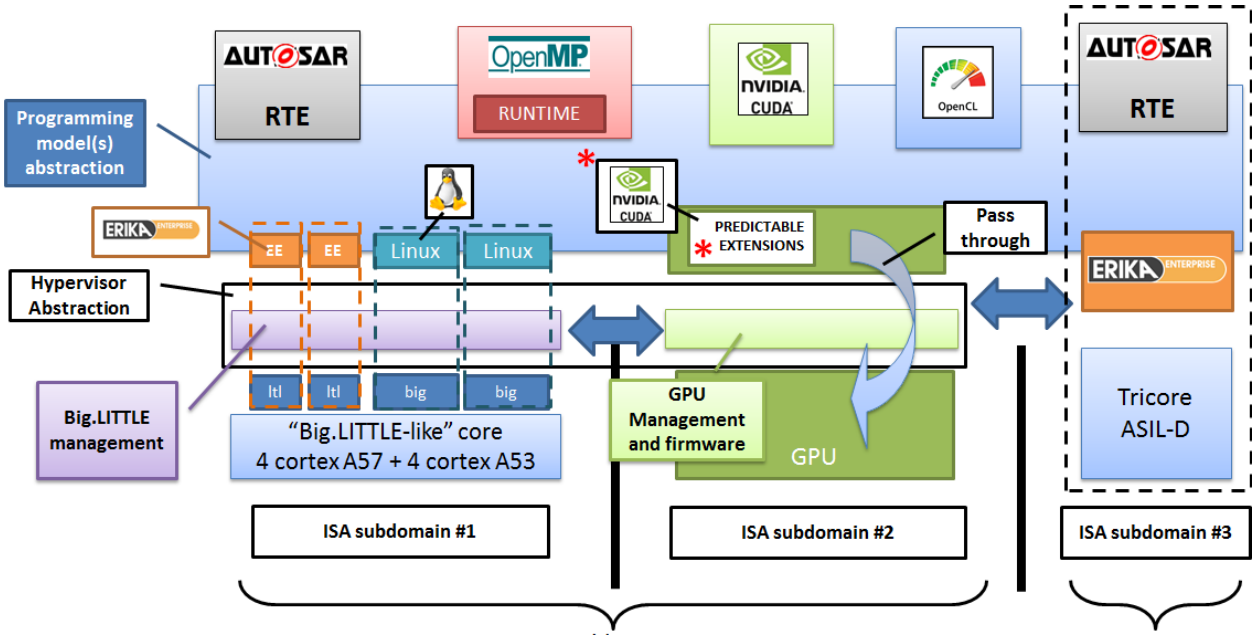


Figure 6: The Hercules Software Stack.

**Memory-centric design**.

In order to achieve predictable execution on heterogeneous many-core platforms, it is necessary to control the way how individual CPU cores and on-chip peripherals access the shared resources such as on-chip interconnects and main memory. Of these, the main memory is the slowest one and likely to be the bottleneck. State-of-the-art approaches are inspired by the so-called PRedictable Execution Model (PREM) [94, 95], where the predictability of memory accesses from single software components (tasks) is increased using prefetching techniques and scheduling prefetch bursts from different cores to not interfere with each other.

Under PREM, tasks are split into pairs of memory and computational phases. Figure 7 shows the distribution of memory accesses of an example application task both in PREM and non- PREM models. In a first memory phase, tasks retrieve and copy data from the main memory into the local cache of the core they are executing on, whereas, in the following, computational phase, they elaborate non-preemptively previously cached data. This execution model allows the variability of memory-contention latencies to be greatly reduced, by explicitly controlling memory accesses during memory phases. As such, it allows the overall task execution times to become much more predictable. Addressing single-core systems, a PREM-compliant co-scheduler is proposed granting main-memory access only when the task being executed on the processor is in the computational phase, without incurring memory conflicts.

### 3.8 Machine and Deep Learning

Machine Learning and Deep Learning denote the main trends topics during the past few years. There are many applications that many companies are developing and improving, thanks to the machine and deep learning. Companies and industries around these fields are present in almost every sector of society, since recommendation systems, news filtering, self-driving cars, general elections, analysis of natural language processing, computer vision, object recognition, video games, among many others.

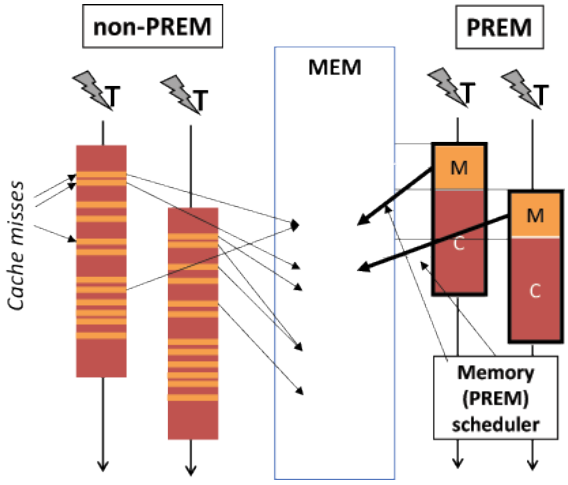


Figure 7: **PR**edictable **E**xecution **M**odel in a parallel environment.

The explosion of machine learning in almost all areas of computing, and more specifically, of deep learning, has been possible due to the improvement in computing hardware such as more powerful GPUs, that have enabled the possibility of investigating artificial neural networks with many hidden layers at a reasonable time (known as deep learning techniques). Along with the hardware, new emerging programming models and programming frameworks such as Google TensorFlow [16], PyTorch [64] have made deep learning accessible for the masses.

Additionally, during the past two years, companies have developed and built specific computing hardware for processing deep learning applications more efficiently. This is the case of Google Tensor Processing Units (TPUs), Tesla AI chips or CEREBRAS's new chip. All of these hardware has been specifically designed for processing deep learning workloads, offering high bandwidth, memory on-chip and very low-latency caches.

### 3.9 Resource Management

A number strategies are put in place towards improving the resource management of heterogeneous computing, considering CPUs, GPUs and FPGAs, and leading to the development of a resource manager whose primary goals is to:

- Serve as a universal orchestrator for heterogeneous resources and acceleration requests.
- Improve scalability and maximize performance of deployed accelerators, ensuring the secure sharing of the available resources.
- Abstract away cumbersome parallel programming languages (e.g. OpenCL) without compromising flexibility.
- Encompass bitstream management and protection capabilities.

An example of such resource manager is Coral [96], which is dedicated to FPGA resources. It is a scalable, reliable and fault-tolerant distributed acceleration system responsible for monitoring, virtualizing and orchestrating clusters of FPGAs. It introduces high-level abstractions by exposing FPGAs as a single pool of accelerators to any application developer that she can easily invoke through simple API calls. Finally, Coral runs as a microservice and is able to run on top of other state-of-the-art resource managers like Hadoop YARN [26] and Kubernetes [27].

Coral Resource manager serves as an abstraction layer on top of the OpenCL runtime system. The OpenCL runtime system is using the drivers from the FPGA vendors and can support multiple kernels in the same FPGA as shown in Figure 8.

Coral provides a straight-forward and simplified API that allows the deployment of the accelerators in the same way as software function calls. That way we avoid complex processes based on OpenCL about the configuration of the bitstreams, the management and the allocation of the buffers and the kernels.

The main advantage is the seamless virtualization of the available resources that it offers. Multiple applications or multi-thread applications can utilize the Coral resource manager by simple invoking the functions that they need to accelerate. Coral enables the sharing of the available FPGA resources when accelerators are requested from multiple applications or threads. Therefore, the software developers can speedup their applications without the complexity of typical heterogeneous platforms.

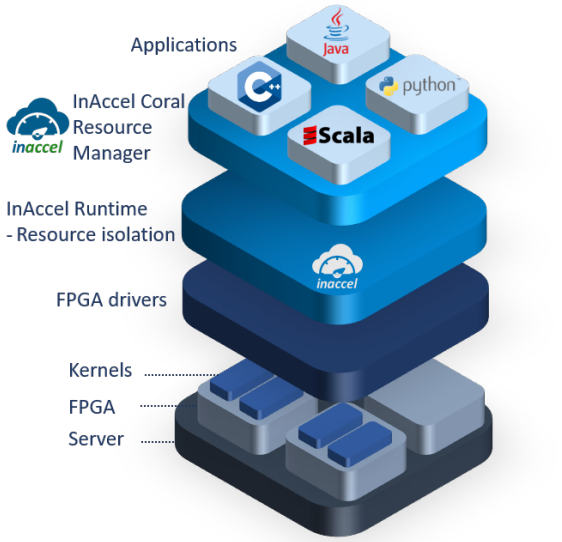


Figure 8: High-level overview of the Coral FPGA resource manager

## 4 Future Research Directions

Heterogeneity is a concept with vast variance, as it is driven by the diversity in the applications' requirements. Therefore, the realm of heterogeneous computing will evolve to support new disruptive applications e.g. Cyber-physical Systems of Systems (CPSoS), Edge/Fog and Cloudlet computing [97, 98], autonomous vehicles [99] as well as HPC systems [100, 101, 102].

Thus, research on heterogeneous systems that satisfy the emerging computing requirements will unveil new challenges across the entire software stack, see Figure 1: from the programming models, to compilers and drivers, middleware and finally to the underlying hardware. These challenges will need to be addressed in a unified manner, that will satisfy the trade-off between compatibility and performance, as discussed in Section 2. Moreover, future heterogeneous computing research will greatly be driven by the emerging trends discussed in Section 3. Due to space limitation, this section will discuss this future research with a focus on resource management and scheduling (Section 4.1), timing predictability (Section 4.2) and programming abstractions (Section 4.3). Other research directions will also be briefly covered (Section 4.4).

### 4.1 Resource Management and Scheduling

In large computing infrastructures the role of managing resources (computing, networking and storage) to schedule tasks (i.e., jobs and services) is played by *orchestrators*. Such components are responsible for configuring, allocating and coordinating the use of a set of resources, being either hardware or software (virtualized resources), to run a certain job or service. Modern orchestrators schedule tasks very quickly on different machines (infrastructure nodes), following a given allocation strategy.

For instance, Figure 9 depicts a typical modern scenario, where highly heterogeneous infrastructure resources are split between data centers (tightly coupled resources), Edge/Fog nodes (distributed resources) and IoT devices, each embedding specialized computing capabilities. In such scenario, the orchestrator receives users' job/service requests through the exposed front-end, and makes decision on the best set of resources used to serve these requests. The decision making generally takes into account multiple criteria, such as maximizing throughput of the whole platform, guaranteeing SLAs [103], minimizing overall energy consumption [104], minimizing the time elapsed for completing the job execution, etc. Decision making is then automatically transformed into an executable workflow, while the resource allocation is done by communicating with local agents. Resource allocation is generally based on feedback information captured by monitoring tools, which is incorporated in the scheduling models used to dynamically allocate the resources. Large effort in this direction is spent to efficiently solving the associated NP-hard scheduling problem [105, 106, 107].

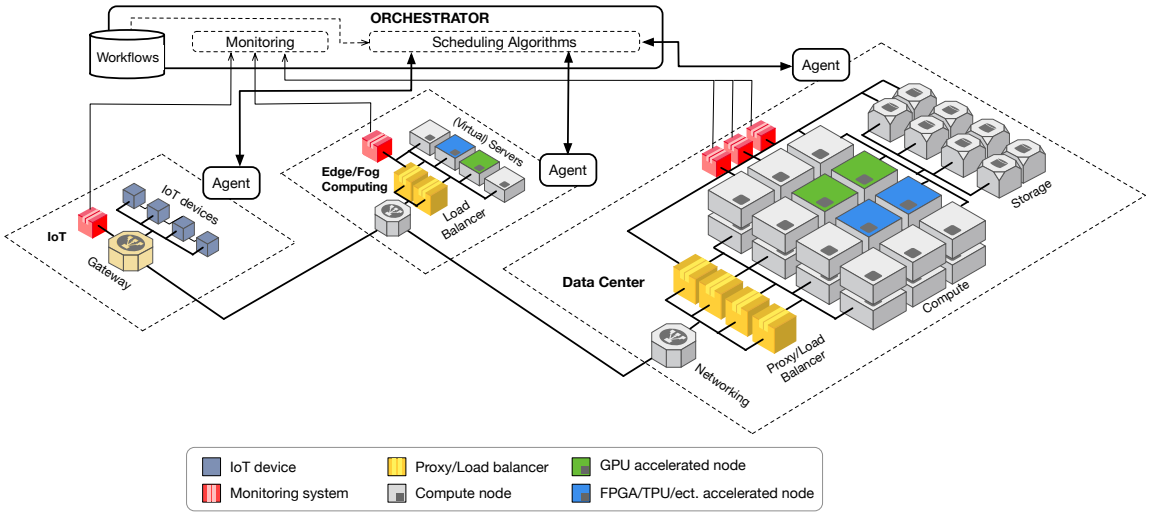


Figure 9: Modern Orchestration scenario across data center, Edge/Fog and IoT resources.

Examples of such conceptual idea can be found in the attempts of extending existing orchestration frameworks [105] and can be recognized in the effort made by EU projects [108, 109, 110].

The orchestrators also provide other advantages, ranging from the capability of auto-scaling used resources for a certain job to offering more flexibility and elasticity in supporting increasing (or decreasing) workload size over time. Also the reliability can take advantage from advanced orchestration strategies. Indeed, the integration of continuous monitoring systems, allows the orchestrator to be aware of actually available resources and thus, in case of failures, re-scheduling the execution of jobs/services on different resources. Looking at future trends, the research directions are many-folds, covering aspects related to a more holistic approaches for energy efficiency (also including the use of AI-based techniques), distributed computing to the edge (including converged HPC, Cloud, AI and Big Data platforms), and management of various forms of hardware acceleration.

Moving towards this direction, one possible new approach could be to make orchestrators less sectorial, considering the management of extremely heterogeneous environments. Heterogeneity, indeed, can be seen from two different points of view: on the one hand, we have the most classic definition of it, i.e., having the integration of different types of architectures (CPU, GPU, FPGA, specialized ASICs, etc.) on the same system bus, with tasks sharing and memory; on the other hand, heterogeneity is represented by environments where computing resources are extended to cover both data center ones and those placed to edge, till the IoT-based sensors (see Figure 9). The majority of the orchestrators are able to manage resources locate on the data center only or, in the other case, resources located only at the edge/fog level; however, a more holistic approach is missing. Indeed, the ICT world is evolving ever faster, going both ways at the same time, with heterogeneous infrastructures that exploit the presence of other different components in the system at different levels. Several contexts of use (in fact) contemplate the use of edge nodes for the management of Big-Data flows coming from IoT devices, to limit the traffic from the latter to the data center. In this case, the presence of an orchestrator able to manage all these resources and the scheduling of jobs/services could allow a better management of the entire system, balancing the use of all the devices involved. On the other hand, focusing on the management of (heterogeneous) resources in the data center, we must mention the birth and proliferation of specific applications for a given domain, requiring specific policies to not negatively affect the performance of such applications. The (probably) most appropriate example in this regard is that of machine learning applications, which are becoming increasingly popular and often require specific hardware because of the necessary computing power demanded. In this context, as in other similar ones, a modern orchestrator should be able to distinguish such applications, allocating the most suitable resources to them, and taking into consideration the way data are generated and exchanged among the jobs/services composing the application. This would allow for better management of existing resources, as well as faster execution times.

Future developments in the orchestration field will also concern the role played by schedulers, especially the strategy followed by these latter to assign resources, whenever the applications are composed by dependent tasks. For instance, the emergence of HPC-as-a-Services (HPCaaS) is towards this direction [111, 112]. Indeed, most of the schedulers rely on very simple allocation strategies, such as allocating tasks in the first available compute nodes (being either a physical node or a virtual machine), thereby verifying only the feasibility of the whole allocation schema. In general,

a feasible node is a node with sufficient resources than can host the task to be performed. However, the problem of allocating resources for a given service or job, can also be seen as an optimization problem. In this case the strategy used, should find the best possible node (not just the first one available) based on multiple criteria (e.g., reducing the number of active nodes, saturating the running machines, minimizing data movement, etc.).

### 4.2 Timing predictability

As platform heterogeneity comes into play, the inherent architectural complexity of the system harnesses the timing predictability of the overall real-time systems. As explained in Section 3.7, current state-of-the-art approaches tackle this by adequately mitigating the shared interference of multiple computing engines to the shared resources, such as the main memory. While researchers have not found how to tackle this problem, in a holistic manner, current results are promising and encouraging to push further efforts towards this direction.

However, this problem refers to the lowest level of a heterogeneous computing stack. Hence, a possible solution would act as basics to raise up the abstraction, and focus on the upper levels of the stack. Indeed, being able to hide and master the complexity of underlying hardware, for instance, via adequate software constructs ) is paramount to make predictability not only *possible*, but also *effective*, while not tackling system programmability. This is done not only with "syntactic sugar" constructs to programming language, but we also advise a new generation of programming models tailored for heterogeneity. For this reason, frontier researchers are devising advanced programming models to represent this crucial aspect at an adequate abstraction level, to let software programmers exploit the tremendous potential of heterogeneous platforms, in a predictable manner.

Real-time systems is a separate group within the spectrum of heterogeneous systems, due to their *critical* nature. Applications running on real-time systems have key critical features, which undergo some kind of certification through safety assessment (hard RT) or performance/QoS assessment (soft or firm RT). In firm RT systems, few/sporadic deadline misses are tolerable, and the result of the computation is basically usefulness. For example, modern automotive systems are increasingly adopting centralized Electrical/Electronic (E/E) architectures where numerous heterogeneous applications at mixed criticality, co-exist on the same *domain controller* ECU. System/integration engineers shall master this design challenge, thereby requiring for expressive performance models capturing the heterogeneity of the hardware-software system. One of the prominent modeling frameworks, which we use as an example, is Amalthea [113]. Amalthea is widely adopted in the automotive domain, whereas, engineers from avionics and other domains might adopt different models based on Matlab/Simulink, Time-Triggered Architecture [114] or Logical-Execution Time (LET) [115]. All of the observations ad ideas introduced in this work can be also applied to these frameworks.

Amalthea is an established modelling tool with a modelling format that interfaces with various commercial tools (e.g., the AUTOSAR automotive standard). This easy plug-and-play feature constitutes Amalthea as a suitable modeling framework not only for academic, but also for industrial research. As a result, engineers are able to model multiple real-time application components, and profile their timing behaviour to provide a predictability assessment.

However, like other modelling tools, Amalthea lacks of the necessary expressiveness to model also complex heterogeneous hardware. Therefore, the ability to model the software and hardware features of highly-parallel embedded accelerators (e.g., GPGPUs [116]) is paramount to integrate and exploit such platforms in the domain of real-time computing.

### 4.3 Programming abstractions

We have shown that practically every new computing system is a combination of heterogeneous components and devices that can be used for accelerating specific types of workloads. Perhaps, in a few years we can have laptops and mobiles devices composed of multi-cores, GPUs, FPGAs and custom accelerators such as Tensor Cores, machine learning dedicated chips, or even quantum devices. The FPGA components are interesting because they can be used to dynamically adapt and execute tasks that can benefit from pipeline-parallelism, while GPUs can be used for solving data intensive applications with a high-volume of operations per work-item.

In Section 3.2 we discussed many emerging programming abstractions, including language's tools, libraries and compilers to use current heterogeneous systems. However, it seems that novel accelerators and customized hardware, appear in accordance with a customized set of tools and programming models. For instance, more than 200s parallel programming models were created during 1990s [117], in a decade that hardware specialization was not a requirement to build more efficient processors.

In recent years, this trend has changed, as computers comprise multiple diverse hardware components. Therefore, there is a trend to facilitate heterogeneous programming from mainstream programming languages, rather than creating

new abstractions. Consequently, software programmers have more options to obtain higher performance and energy efficiency for the execution of their applications.

However, to make the execution scalable and offer the usage of new accelerators for mass software execution, it is still necessary the programmers to build customized abstractions to facilitate software maintenance.

This is a source of a trade-off between creating high-performing applications, and the ability to apply quick changes to evolve and adapt fast to new hardware and new technologies.

Current trends show that new parallel and heterogeneous programming models will still emerge. However, to make them usable and comprehensive for many fields and sectors, converging is also a requirement. Currently, there are some examples that showcase some initial efforts towards this direction. For example, Intel is expected to release a new API (called oneAPI) for targeting all heterogeneous hardware within the same C++ programs; Intel oneAPI includes compilers for multi-cores, Intel integrated GPUs, and Intel FPGAs. Along the same direction of Intel oneAPI, SYCL is another parallel programming abstraction with the aim to automatically bring heterogeneous computing with existing constructions in the C++ programming language. The idea behind these parallel programming models is that developers can program, within the same source, CPU as well as GPU/FPGA code and still be standard C++ code. We foresee more programming models along this line, in which the code to be accelerated is codified at the same level and style as the main programming language.

### 4.4 Other Research Directions

Significant research is already in place to address heterogeneous computing technological and adoption challenges. The future research and development agenda will greatly be driven by the emerging trends discussed in Section 3. Next, other key future directions are briefly introduced.

**Design-Time Tooling**. As heterogeneity is driven by the diversity in the applications, software and hardware, it is imperative to have a research agenda on future design-time tools to support how best to achieve an optimal placement of software tasks in a given heterogeneous hardware environment.

The importance of the availability of such tools throughout the design exploration process is paramount: they will aim to facilitate the exploitation of heterogeneous hardware platforms by automating the exploration of design "variants" when compiling a software task, and at the same time characterise performance time and energy. Such tools will determine what software components would benefit most from processing on specific heterogeneous hardware and will also explore: 1) what-if scenarios in order to benefit the overall application execution, and 2) the optimal placement and scheduling of tasks to achieve the desired trade-off between e.g. performance and energy consumption.

**Reliability**. Reliability in heterogeneous computing systems is a major concern for all stake holders, e.g. end-users, application developers, application providers. With heterogeneity expanding further in the future, it will be imperative to keep assessing or predicting the reliability of applications operating in heterogeneous computing systems. Ensuring these systems' reliability in turns requires examining reliability of each individual component or factors involved in applications before predicting or assessing reliability of the whole system. Due to the complexity of such system, this will require implementing novel, transparent fault detection and fault recovery schemes to provide seamless interaction to end-users.

**Sustainability** Sustainability of ICT systems has attracted considerable attention due to the energy consumption of such systems. Cyber Physical Systems and the IoT are discovering potential demand domains where relatively high performance is required from systems which by the nature of the domain are physically constrained, by size, weight or energy dissipation, or by the reliance on battery or solar energy. Examples include vehicles where space, weight, heat dissipation and reliance on the engine for power are all constraints. Other examples include other land, underwater and air vehicles, including unmanned drones.

However, even when physical constraints do not apply, for all kinds of workloads, heterogeneous systems might handle the workload with fewer and/or smaller servers, saving money, space and energy. Such systems can slash the energy used to run certain applications, which helps gain clear benefits and addresses the growing interest in green solutions and the pressure to reduce the environmental impact of, e.g. data centres. A common theme across all scenarios is the need for low-power computing systems that are fully interconnected, self-aware, context-aware and self-optimising within application boundaries. Also, increased greenhouse gas emissions are driving the need to lower carbon footprints and deploy more renewable - green energy sources.

There are a number of initiatives to address sustainability in heterogeneous computing, e.g. novel hardware based sleep-start controls and clock speed management techniques in multi-core architectures; dynamically coupling the flow of energy to computing and communication resources; the application of machine learning for task allocation

and scheduling to optimises a prescribed performance profile; the consideration of the reduced access distance and network size from the end-user's application to edge computing devices as it has the potential to create energy savings in networks, but much more work will be needed.

**Security and Privacy** Security enforcement (and privacy) are of paramount importance in heterogeneous computing. Security however is a complex notion due to the specificity of environment (e.g. IoT, embedded, cloud), the context-specific meaning, the application-specific requirements or stakeholder-specific perceptions. Security threats need to be identified in the context of the applications running on heterogeneous hardware and contingency plans provided in the form of end-to-end security mechanisms applicable for applications running in such environments. Note that reducing the architecture complexity may be required to guarantee security.

A future direction will be to investigate optimal synergies between hardware security mechanisms and software (at all levels, including the Operating System, libraries and user code). The close coordination of hardware and software mechanisms ensures that the cost of the security mechanisms is minimized. For example, the Instruction Set Randomization (ISR) mechanism itself is part of the processor architecture, but significant code needs to be added to the Operating System to fully exploit such mechanism.

## 5 Summary and Conclusions

Heterogeneous computing has revolutionised the computer science horizon during the past decade and enabled the emergence of a number of challenges ahead. The next decade will bring about significant new requirements, from Cyber Physical Systems and Systems, Industrial IoT and Cloud data centres producing very large data streams to store, manage, and analyse, to energy and cost-aware personalised computing services that must adapt to a plethora of heterogeneous hardware devices while optimising for multiple criteria including application-level QoS constraints. These requirements will be posing several new challenges and will be creating the need for new approaches and research strategies, and a re-evaluation of not only the traditional software stack (construction, deployment, operation) but issues such as scalability, resource provisioning, and security.

After identifying the main components of the heterogeneous computing paradigm (see Figure 1), this comprehensive manifesto brought the advancements together and proposed the challenges still to be addressed in realising the future generation heterogeneous computing. In the process, the manifesto identified the current major challenges in heterogeneous computing domain and summarised the state-of-the-art along with the limitations. The manifesto also discussed the emerging trends and impact areas that further drive these heterogeneous computing challenges. Having identified these open issues, the manifesto then offered comprehensive future research directions in the horizon for the next decade. The discussed directions show a promising and exciting future for heterogeneous computing field from the perspective of research and development, and the manifesto calls the research community for action in addressing them.

## References


[1] Amazon EC2 F1 Instances, 2019. https://aws.amazon.com/ec2/instance-types/f1/.

[2] Cloud TPU, 2019. https://cloud.google.com/tpu/.

[3] K. Djemame, D. Armstrong, R. Kavanagh, J.C Deprez, A.J. Ferrer, D.G. Perez, R. Badia, R. Sirvent, J. Ejarque, and Y. Georgiou. Tango: Transparent heterogeneous hardware architecture deployment for energy gain in operation. In S. Tamarit, G. Vigueras, M. Carro, and J. Marino, editors, *Proceedings of the First Workshop on Program Transformation for Programmability in Heterogeneous Architectures*, Barcelona, Spain, March 2016. http://arxiv.org/pdf/1603.01407.

[4] Allied market research, 2019. https://www.alliedmarketresearch.com/.

[5] Jeffrey Dean and Sanjay Ghemawat. Mapreduce: Simplified data processing on large clusters. In *OSDI'04: Sixth Symposium on Operating System Design and Implementation*, pages 137–150, San Francisco, CA, 2004.

[6] Murray Cole. *Algorithmic Skeletons: Structured Management of Parallel Computation*. MIT Press, Cambridge, MA, USA, 1991.

[7] R R Springmeyer, C. Still, Martin Schulz, Jill Ahrens, Karl Scott Hemmert, Ron Minnich, Pat McCormick, Lorrae Ward, and Diana Knoll. From petascale to exascale: Eight focus areas of rd challenges for hpc simulation environments. 2011.

[8] OpenACC-Standard.org. The OpenACC Application Programming Interface 1.0, November 2011.

[9] OpenMP Architecture Review Board. OpenMP application program interface version 4.0, July 2013.

[10] Alejandro Duran, Eduard Ayguadé, Rosa M. Badia, Jesús Labarta, Luis Martinell, Xavier Martorell, and Judit Planas. Ompss: a proposal for programming heterogeneous multi-core architectures. *Parallel Processing Letters*, 21:173–193, 2011.

[11] Message P Forum. Mpi: A message-passing interface standard. Technical report, Knoxville, TN, USA, 1994.

[12] Jeffrey Dean and Sanjay Ghemawat. Mapreduce: Simplified data processing on large clusters. In *OSDI'04: Sixth Symposium on Operating System Design and Implementation*, pages 137–150, San Francisco, CA, 2004.

[13] Henrik Nilsson, Antony Courtney, and John Peterson. Functional reactive programming, continued. In *Proceedings of the 2002 ACM SIGPLAN Workshop on Haskell*, Haskell '02, pages 51–64, New York, NY, USA, 2002. ACM.

[14] Nvidia CUDA, 2007. `http://developer.nvidia.com/`.

[15] OpenCL, 2009. `http://www.khronos.org/opencl/`.

[16] Martín Abadi, Ashish Agarwal, Paul Barham, Eugene Brevdo, Zhifeng Chen, Craig Citro, Greg Corrado, Andy Davis, Jeffrey Dean, Matthieu Devin, Sanjay Ghemawat, Ian Goodfellow, Andrew Harp, Geoffrey Irving, Michael Isard, Yangqing Jia, Rafal Jozefowicz, Lukasz Kaiser, Manjunath Kudlur, Josh Levenberg, Dan Mané, Rajat Monga, Sherry Moore, Derek Murray, Chris Olah, Mike Schuster, Jonathon Shlens, Benoit Steiner, Ilya Sutskever, Kunal Talwar, Paul Tucker, Vincent Vanhoucke, Vijay Vasudevan, Fernanda Viégas, Oriol Vinyals, Pete Warden, Martin Wattenberg, Martin Wicke, Yuan Yu, and Xiaoqiang Zheng. Tensorflow: Large-scale machine learning on heterogeneous distributed systems, 2015.

[17] Ruyman Reyes and Victor Lomüller. Sycl: Single-source c++ accelerator programming. In *PARCO*, 2015.

[18] AMD. Aparapi, 2016. `http://aparapi.github.io/`.

[19] K. Ishizaki, A. Hayashi, G. Koblents, and V. Sarkar. Compiling and Optimizing Java 8 Programs for GPU Execution. In *2015 International Conference on Parallel Architecture and Compilation (PACT)*, pages 419–431, Oct 2015.

[20] Sumtra. Sumatra OpenJDK, 2015. `http://openjdk.java.net/projects/sumatra/`.

[21] Christopher J. Rossbach, Yuan Yu, Jon Currey, Jean-Philippe Martin, and Dennis Fetterly. Dandelion: A compiler and runtime for heterogeneous systems. In *Proceedings of the Twenty-Fourth ACM Symposium on Operating Systems Principles*, SOSP '13, pages 49–68, New York, NY, USA, 2013. ACM.

[22] Naila Farooqui, Christopher J. Rossbach, Yuan Yu, and Karsten Schwan. Leo: A profile-driven dynamic optimization framework for gpu applications. In *Proceedings of the 2014 International Conference on Timely Results in Operating Systems*, TRIOS'14, pages 5–5, Berkeley, CA, USA, 2014. USENIX Association.

[23] Dirk Koch, Frank Hannig, and Daniel Ziener. *FPGAs for Software Programmers*. Springer Publishing Company, Incorporated, 1st edition, 2016.

[24] R. Nane, V. Sima, C. Pilato, J. Choi, B. Fort, A. Canis, Y. T. Chen, H. Hsiao, S. Brown, F. Ferrandi, J. Anderson, and K. Bertels. A Survey and Evaluation of FPGA High-Level Synthesis Tools. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2016.

[25] O. Arcas-Abella, G. Ndu, N. Sonmez, M. Ghasempour, A. Armejach, J. Navaridas, Wei Song, J. Mawer, A. Cristal, and M. Luján. An Empirical Evaluation of High-Level Synthesis Languages and Tools for Database Acceleration. In *24th International Conference on Field Programmable Logic and Applications (FPL)*, 2014.

[26] Apache hadoop yarn, Sep 2019. https://hadoop.apache.org/docs/current/hadoop-yarn/hadoop-yarn-site/YARN.html.

[27] Kubernetes. production-grade container orchestration., 2020. https://kubernetes.io/.

[28] O. Terzo, K. Djemame, A. Scionti, and C. Pezuela. *Heterogeneous Computing Architectures: Challenges and Vision*. CRC Press, 1st edition, 2019.

[29] Chris Cummins, Pavlos Petoumenos, Zheng Wang, and Hugh Leather. End-to-end deep learning of optimization heuristics. In *PACT*. ACM, 2017.

[30] Chris Cummins, Pavlos Petoumenos, Zheng Wang, and Hugh Leather. Synthesizing benchmarks for predictive modeling. In *Proceedings of the 2017 International Symposium on Code Generation and Optimization*, CGO '17, page 86–99. IEEE Press, 2017.

[31] Zheng Wang, Dominik Grewe, and Michael F. P. O'boyle. Automatic and portable mapping of data parallel programs to opencl for gpu-based heterogeneous systems. *ACM Trans. Archit. Code Optim.*, 11(4), December 2014.

[32] R. Cavicchioli, N. Capodieci, and M. Bertogna. Memory interference characterization between cpu cores and integrated gpus in mixed-criticality platforms. In *2017 22nd IEEE International Conference on Emerging Technologies and Factory Automation (ETFA)*, pages 1–10, Sep. 2017.

[33] K. Djemame, R. Kavanagh, D. Armstrong, R. Sirvent, J. Ejarque, F. Lordan, M. Macias, J. Guitart, and R.M. Badia. Energy efficiency support through intra-layer cloud stack adaptation. In J. Altmann, editor, *13th International Conference on Economics of Grids, Clouds, Systems and Services (GECON 2016)*. Springer, September 2016.

[34] R. Kavanagh, K. Djemame, J. Ejarque, R.M. Badia, and D. Garcia-Perez. Energy-aware self-adaptation for application execution on heterogeneous parallel architectures. *IEEE Transactions on Sustainable Computing Systems*, 2019.

[35] Spark-T4 Processor, 2010. http://www.oracle.com/us/products/servers-storage/servers/sparc-enterprise/t-series/sparc-t4-processor-ds-497205.pdf.

[36] Shay Gueron. Intel White paper - Advanced Encryption Standard (AES) Instructions Set, 2008. http://ferretronix.com/unigroup/intel_aes_ni/aes-instructions-set_wp.pdf.

[37] Christian Collberg and Jasvir Nagra. *Surreptitious Software: Obfuscation, Watermarking, and Tamperproofing for Software Protection*. Addison-Wesley Professional, 1st edition, 2009.

[38] Benjamin Lynn, Manoj Prabhakaran, and Amit Sahai. Positive results and techniques for obfuscation. In Christian Cachin and Jan L. Camenisch, editors, *Advances in Cryptology - EUROCRYPT 2004*, pages 20–39, Berlin, Heidelberg, 2004. Springer Berlin Heidelberg.

[39] L. Davi, M. Hanreich, D. Paul, A. Sadeghi, P. Koeberl, D. Sullivan, O. Arias, and Y. Jin. Hafix: Hardware-assisted flow integrity extension. In *52nd ACM/EDAC/IEEE Design Automation Conference (DAC)*, 2015.

[40] Nick Christoulakis, George Christou, Elias Athanasopoulos, and Sotiris Ioannidis. Hcfi: Hardware-enforced control-flow integrity. CODASPY '16, 2016.

[41] Ruan de Clercq and Ingrid Verbauwhede. A survey of hardware-based control flow integrity (cfi), 2017.

[42] Yier Jin, Dean Sullivan, Orlando Arias, Ahmad-Reza Sadeghi, and Lucas Davi. *Hardware Control Flow Integrity*. Association for Computing Machinery and Morgan Claypool, 2018.

[43] Gaurav S. Kc, Angelos D. Keromytis, and Vassilis Prevelakis. Countering code-injection attacks with instruction-set randomization. CCS '03. Association for Computing Machinery, 2003.

[44] Antonis Papadogiannakis, Laertis Loutsis, Vassilis Papaefstathiou, and Sotiris Ioannidis. Asist: Architectural support for instruction set randomization. CCS '13. Association for Computing Machinery, 2013.

[45] S. Du, H. Shu, F. Kang, X. Xiong, and Z. Wang. Hardware-based instruction set randomization against code injection attacks. In *2017 3rd IEEE International Conference on Computer and Communications (ICCC)*, 2017.

[46] K. Sinha, V. P. Kemerlis, and S. Sethumadhavan. Reviving instruction set randomization. In *2017 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2017.

[47] Ana Nora Sovarel, David Evans, and Nathanael Paul. "Where's the FEEB? The Effectiveness of Instruction Set Randomization", 2005.

[48] Intel Software Guard Extensions, 2020. https://software.intel.com/content/www/us/en/develop/topics/software-guard-extensions.html.

[49] Arm TrustZone Technology, 2020. https://developer.arm.com/ip-products/security-ip/trustzone.

[50] Henk Van Tilborg and Sushil Jajodia. "Encyclopedia of Cryptography and Security", 2011.

[51] Javier Navaridas, Josh Lant, Jose A. Pascual, Mikel Luján, and John Goodacre. Design exploration of multi-tier interconnection networks for exascale systems. In *Proceedings of the 48th International Conference on Parallel Processing*, ICPP'2019, New York, NY, USA, 2019. ACM.

[52] I. Mavroidis et al. ECOSCALE: reconfigurable computing and runtime system for future exascale systems. In *2016 Design, Automation & Test in Europe Conference & Exhibition, DATE 2016, Dresden, Germany, March 14-18, 2016*, pages 696–701, 2016.

[53] F. A. Escobar, X. Chang, and C. Valderrama. Suitability analysis of fpgas for heterogeneous platforms in hpc. *IEEE Transactions on Parallel and Distributed Systems*, 27(2):600–612, Feb 2016.

[54] Michaela Blott. Reconfigurable future for hpc. In *2016 International Conference on High Performance Computing Simulation (HPCS)*, pages 130–131, July 2016.

[55] Alessandro Cilardo. Htcomp: bringing reconfigurable hardware to future high-performance applications. *IJHPCN*, 12(1):74–83, 2018.

[56] Ryohei Kobayashi, Yuma Oobata, Norihisa Fujita, Yoshiki Yamaguchi, and Taisuke Boku. Opencl-ready high speed FPGA network for reconfigurable high performance computing. In *Proceedings of the International Conference on High Performance Computing in Asia-Pacific Region, HPC Asia 2018, Chiyoda, Tokyo, Japan, January 28-31, 2018*, pages 192–201, 2018.

[57] Jason Cong, Zhenman Fang, Michael Lo, Hanrui Wang, Jingxian Xu, and Shaochong Zhang. Understanding performance differences of fpgas and gpus. pages 93–96, 04 2018.

[58] Tomislav Matic, Ivan Aleksi, and Zeljko Hocenski. Cpu, gpu and fpga implementations of mald: Ceramic tile surface defects detection algorithm. *Automatika*, 55, 02 2014.

[59] Pingfan Meng, Matt Jacobsen, Motoki Kimura, Vladimir Dergachev, Thomas Anantharaman, Michael Requa, and Ryan Kastner. Hardware accelerated novel optical de novo assembly for large-scale genomes. pages 1–8, 09 2014.

[60] Eriko Nurvitadhi, Gabriel Weisz, Yu Wang, Skand Hurkat, Marie Nguyen, James Hoe, Jose Martinez, and Carlos Guestrin. Graphgen: An fpga framework for vertex-centric graph computation. pages 25–28, 05 2014.

[61] TIOBE. TIOBE Index. `https://www.tiobe.com/tiobe-index/`, 2019. [Online; accessed May 2019].

[62] IEEE. IEEE Spectrum: The 2018 Top Programming Languages. `https://spectrum.ieee.org/at-work/innovation/the-2018-top-programming-languages`, 2018. [Online; accessed May 2019].

[63] Martin Abadi, Paul Barham, Jianmin Chen, Zhifeng Chen, Andy Davis, Jeffrey Dean, Matthieu Devin, Sanjay Ghemawat, Geoffrey Irving, Michael Isard, Manjunath Kudlur, Josh Levenberg, Rajat Monga, Sherry Moore, Derek G. Murray, Benoit Steiner, Paul Tucker, Vijay Vasudevan, Pete Warden, Martin Wicke, Yuan Yu, and Xiaoqiang Zheng. Tensorflow: A system for large-scale machine learning. In *12th USENIX Symposium on Operating Systems Design and Implementation (OSDI 16)*, pages 265–283, 2016.

[64] PyTorch, 2020. https://pytorch.org/.

[65] Juan Fumero, Michail Papadimitriou, Foivos S. Zakkak, Maria Xekalaki, James Clarkson, and Christos Kotselidis. Dynamic application reconfiguration on heterogeneous hardware. In *Proceedings of the 15th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments*, VEE 2019, pages 165–178, New York, NY, USA, 2019. ACM.

[66] James Clarkson, Juan Fumero, Michail Papadimitriou, Foivos S. Zakkak, Maria Xekalaki, Christos Kotselidis, and Mikel Luján. Exploiting high-performance heterogeneous hardware for java programs using graal. In *Proceedings of the 15th International Conference on Managed Languages & Runtimes*, ManLang '18, pages 4:1–4:13, New York, NY, USA, 2018. ACM.

[67] Juan Fumero. *Accelerating Interpreted Programming Languages on GPUs with Just-In-Time and Runtime Optimisations*. PhD thesis, The University of Edinburgh, UK, August 2017.

[68] Juan Fumero, Michel Steuwer, Lukas Stadler, and Christophe Dubach. Just-In-Time GPU Compilation for Interpreted Languages with Partial Evaluation. In *Proceedings of the 13th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments*, VEE '17, pages 60–73, New York, NY, USA, 2017. ACM.

[69] Dejice Jacob and Jeremy Singer. Alpyna: Acceleration of loops in python for novel architectures. In *Proceedings of the 6th ACM SIGPLAN International Workshop on Libraries, Languages and Compilers for Array Programming*, ARRAY 2019, pages 25–34, New York, NY, USA, 2019. ACM.

[70] Dejice Jacob, Phil Trinder, and Jeremy Singer. Python programmers have gpus too: Automatic python loop parallelization with staged dependence analysis. In *Proceedings of the 15th ACM SIGPLAN International Symposium on Dynamic Languages*, DLS 2019, pages 42–54, New York, NY, USA, 2019. ACM.

[71] Mohaned Qunaibit, Stefan Brunthaler, Yeoul Na, Stijn Volckaert, and Michael Franz. Accelerating Dynamically-Typed Languages on Heterogeneous Platforms Using Guards Optimization. In Todd Millstein, editor, *32nd European Conference on Object-Oriented Programming (ECOOP 2018)*, volume 109 of *Leibniz International Proceedings in Informatics (LIPIcs)*, pages 16:1–16:29, Dagstuhl, Germany, 2018. Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik.

[72] Stelios Mavridis, Manolis Pavlidakis, Ioannis Stamoulias, Christos Kozanitis, Nikolaos Chrysos, Christoforos Kachris, Dimitrios Soudris, and Angelos Bilas. Vinetalk: Simplifying software access and sharing of fpgas in datacenters. In *Field Programmable Logic and Applications (FPL), 2017 27th International Conference on*, pages 1–4. IEEE, 2017.

[73] ICS FORTH. Gpu sharing across multiple concurent applications. https://github.com/vineyard2020/vinetalkSuite, 2018.

[74] Raffaele Montella, Sokol Kosta, David Oro, Javier Vera, Carles Fernández, Carlo Palmieri, Diana Di Luccio, Giulio Giunta, Marco Lapegna, and Giuliano Laccetti. Accelerating linux and android applications on low-power devices through remote gpgpu offloading. *Concurrency and Computation: Practice and Experience*, 29(24):e4286, 2017.

[75] Jorge Albericio, Patrick Judd, Tayler Hetherington, Tor Aamodt, Natalie Enright Jerger, and Andreas Moshovos. Cnvlutin: Ineffectual-neuron-free deep neural network computing. In *Computer Architecture (ISCA), 2016 ACM/IEEE 43rd Annual International Symposium on*, 2016.

[76] Jeffrey Dean and Luiz André Barroso. The tail at scale. *Commun. ACM*, 56(2):74–80, February 2013.

[77] Sreepathi Pai, Matthew J. Thazhuthaveetil, and R. Govindarajan. Improving gpgpu concurrency with elastic kernels. In *Proceedings of the Eighteenth International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS '13, pages 407–418, New York, NY, USA, 2013. ACM.

[78] Quan Chen, Hailong Yang, Jason Mars, and Lingjia Tang. Baymax: Qos awareness and increased utilization for non-preemptive accelerators in warehouse scale computers. In *Proceedings of the Twenty-First International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS '16, pages 681–696, New York, NY, USA, 2016. ACM.

[79] Zhengwei Qi, Jianguo Yao, Chao Zhang, Miao Yu, Zhizhou Yang, and Haibing Guan. Vgris: Virtualized gpu resource isolation and scheduling in cloud gaming. *ACM Trans. Archit. Code Optim.*, 11(2):17:1–17:25, July 2014.

[80] NVIDIA. Whitepaper pascal compute preemption. https://images.nvidia.com/content/pdf/tesla/whitepaper/pascal-architecture-whitepaper.pdf, 2016. Online; accessed 25 July 2016.

[81] Panagiotis Garefalakis, Konstantinos Karanasos, and Peter Pietzuch. Neptune: Scheduling suspendable tasks for unified stream/batch applications. In *Proceedings of the Third ACM Symposium on Cloud Computing (SoCC'19)*.

[82] Ramon Amela, Cristian Ramon-Cortes, Jorge Ejarque, Javier Conejero, and Rosa M Badia. Enabling Python to Execute Efficiently in Heterogeneous Distributed Infrastructures with PyCOMPSs. In *Proceedings of the 7th Workshop on Python for High-Performance and Scientific Computing*, PyHPC'17, pages 1:1—-1:10, New York, NY, USA, 2017. ACM.

[83] Karim Djemame, Richard Kavanagh, Vasilios Kelefouras, Adrià Aguilà, Jorge Ejarque, Rosa M Badia, David García Pérez, Clara Pezuela, Lotfi Deprez, Jean-Christophe Guedria, Renaud De Landtsheer, and Yiannis Georgiou. Towards an Energy-Aware Framework for Application Development and Execution in Heterogeneous Parallel Architectures. In *Hardware Accelerators in Data Centers*, chapter 7. Springer International Publishing, 2018.

[84] Z Hou, Z Zhao, W Sheng, and W He. System level power consumption modeling and optimization for coarse-grained reconfigurable architectures. In *2016 International Conference on Integrated Circuits and Microsystems (ICICM)*, pages 1–6, nov 2016.

[85] Kizheppatt Vipin and Suhaib A Fahmy. FPGA Dynamic and Partial Reconfiguration: A Survey of Architectures, Methods, and Applications. *ACM Comput. Surv.*, 51(4):72:1—-72:39, jul 2018.

[86] Christian Krupitzer, Felix Maximilian Roth, Sebastian VanSyckel, Gregor Schiele, and Christian Becker. A survey on engineering approaches for self-adaptive systems. *Pervasive and Mobile Computing*, 17:184 – 206, 2015.

[87] NVIDIA. Jetson AGX Xavier Developer Kit, 2018.

[88] NVIDIA. Jetson TX2 Module, 2017.

[89] NVIDIA. NVIDIA DRIVE PX: scalable AI Supercomputer For Autonomous Driving, 2017.

[90] Ignacio Sañudo, Roberto Cavicchioli, Nicola Capodieci, Paolo Valente, and Marko Bertogna. A survey on shared disk i/o management in virtualized environments under real time constraints. *SIGBED Rev.*, 15(1):57–63, March 2018.

[91] Rohan Tabish, Renato Mancuso, Saud Wasly, Rodolfo Pellizzoni, and Marco Caccamo. A real-time scratchpad-centric OS with predictable inter/intra-core communication for multi-core embedded systems. *Real-Time Systems*, 55(4):850–888, 2019.

[92] Joel Matejka, Björn Forsberg, Michal Sojka, Přemysl Šůcha, Luca Benini, Andrea Marongiu, and Zdeněk Hanzálek. Combining prem compilation and static scheduling for high-performance and predictable mpsoc execution. *Parallel Computing*, 85:27 – 44, 2019.

[93] The Hercules Consortium. Hercules – High-Performance Real-time Architectures for Low-Power Embedded Systems.

[94] R. Pellizzoni, E. Betti, S. Bak, G. Yao, J. Criswell, M. Caccamo, and R. Kegley. A predictable execution model for cots-based embedded systems. In *2011 17th IEEE Real-Time and Embedded Technology and Applications Symposium*, pages 269–279, April 2011.

[95] P. Burgio, A. Marongiu, P. Valente, and M. Bertogna. A memory-centric approach to enable timing-predictability within embedded many-core accelerators. In *2015 CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST)*, pages 1–8, Oct 2015.

[96] Cora fpga resource manager. https://www.inaccel.com/, 2019.

[97] Sparsh Mittal. A survey on optimized implementation of deep learning models on the nvidia jetson platform. *Journal of Systems Architecture*, 2019.

[98] Stephen Cass. Taking ai to the edge: Google's tpu now comes in a maker-friendly package. *IEEE Spectrum*, 56(5):16–17, 2019.

[99] Chang-song Oh and Jong-min Yoon. Hardware acceleration technology for deep-learning in autonomous vehicles. In *2019 IEEE International Conference on Big Data and Smart Computing (BigComp)*, pages 1–3. IEEE, 2019.

[100] Satoshi Matsubara, Motomu Takatsu, Toshiyuki Miyazawa, Takayuki Shibasaki, Yasuhiro Watanabe, Kazuya Takemoto, and Hirotaka Tamura. Digital annealer for high-speed solving of combinatorial optimization problems and its applications. In *2020 25th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 667–672. IEEE, 2020.

[101] Amran A Al-Aghbari and Muhammad ES Elrabaa. Cloud-based fpga custom computing machines for streaming applications. *IEEE Access*, 7:38009–38019, 2019.

[102] David Ojika, Ann Gordon-Ross, Herman Lam, and Bhavesh Patel. Faam: Fpga-as-a-microservice-a case study for data compression. In *EPJ Web of Conferences*, volume 214, page 07029. EDP Sciences, 2019.

[103] Nikita Sharma and Sudarshan Maurya. Sla-based agile vm management in cloud & datacenter. In *2019 International Conference on Machine Learning, Big Data, Cloud and Parallel Computing (COMITCon)*, pages 252–257. IEEE, 2019.

[104] Alberto Scionti, Klodiana Goga, F Lubrano, and Olivier Terzo. Towards energy efficient orchestration of cloud computing infrastructure. In *Conference on Complex, Intelligent, and Software Intensive Systems*, pages 172–183. Springer, 2018.

[105] Kuljeet Kaur, Sahil Garg, Georges Kaddoum, Syed Hassan Ahmed, and Mohammed Atiquzzaman. Keids: Kubernetes based energy and interference driven scheduler for industrial iot in edge-cloud ecosystem. *IEEE Internet of Things Journal*, 2019.

[106] Seyedehmehrnaz Mireslami, Logan Rakai, Mea Wang, and Behrouz H Far. Dynamic cloud resource allocation considering demand uncertainty. *IEEE Transactions on Cloud Computing*, 2019.

[107] Somnath Mazumdar and Marco Pranzo. Power efficient server consolidation for cloud data center. *Future Generation Computer Systems*, 70:4–16, 2017.

[108] Jochen Martin Eppler, Anne Carstensen, and Dirk Pleiter. Icei/fenix: Hpc and cloud infrastructure for computational neuroscientists. In *NEST Conference 2019*, 2019.

[109] Alberto Scionti, Jan Martinovic, Olivier Terzo, Etienne Walter, Marc Levrier, Stephan Hachinger, Donato Magarielli, Thierry Goubier, Stephane Louise, Antonio Parodi, et al. Hpc, cloud and big-data convergent architectures: The lexis approach. In *Conference on Complex, Intelligent, and Software Intensive Systems*, pages 200–212. Springer, 2019.

[110] Thierry Goubier, Andrea Ajmar, Carmine D'Amico, Paul Dubrulle, Susanna Grita, Stephane Louise, Jan Martinovič, Tomáš Martinovič, Natalja Rakowsky, Paolo Savio, et al. Earthquake and tsunami workflow leveraging the modern hpc/cloud environment in the lexis project. In *International Conference on Network-Based Information Systems*, pages 223–234. Springer, 2019.

[111] Vojtěch Cima, Stanislav Böhm, Jan Martinovič, Jiří Dvorskỳ, Kateřina Janurová, Tom Vander Aa, Thomas J Ashby, and Vladimir Chupakhin. Hyperloom: a platform for defining and executing scientific pipelines in distributed environments. In *Proceedings of the 9th Workshop and 7th Workshop on Parallel Programming and RunTime Management Techniques for Manycore Architectures and Design Tools and Architectures for Multicore Embedded Computing Platforms*, pages 1–6. ACM, 2018.

[112] Vojtech Cima, Stanislav Böhm, Jan Martinovič, Jiří Dvorskỳ, Thomas J Ashby, and Vladimir Chupakhin. Hyperloom possibilities for executing scientific workflows on the cloud. In *Conference on Complex, Intelligent, and Software Intensive Systems*, pages 397–406. Springer, 2017.

[113] An Open Platform Project for Embedded Multicore Systems, 2013.

[114] W. Bin, Z. Yunsheng, X. Xin, and W. Shuai. Time-triggered architecture (tta) in industry hard r-t embedded control software design. In *2007 Chinese Control Conference*, pages 736–739, 2007.

[115] J. Martinez, I. Sañudo, and M. Bertogna. Analytical characterization of end-to-end communication delays with logical execution time. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(11):2244–2254, 2018.

[116] Falk Wurst, Dakshina Dasari, Arne Hamann, Dirk Ziegenbein, Ignacio Sañudo, Nicola Capodieci, Marko Bertogna, and Paolo Burgio. System performance modelling of heterogeneous HW platforms: An automated driving case study. In *22nd Euromicro Conference on Digital System Design, DSD 2019, Kallithea, Greece, August 28-30, 2019*, pages 365–372, 2019.

[117] Paul E. McKenney. Is parallel programming hard, and, if so, what can you do about it? (v2017.01.02a). *CoRR*, abs/1701.00854, 2017.